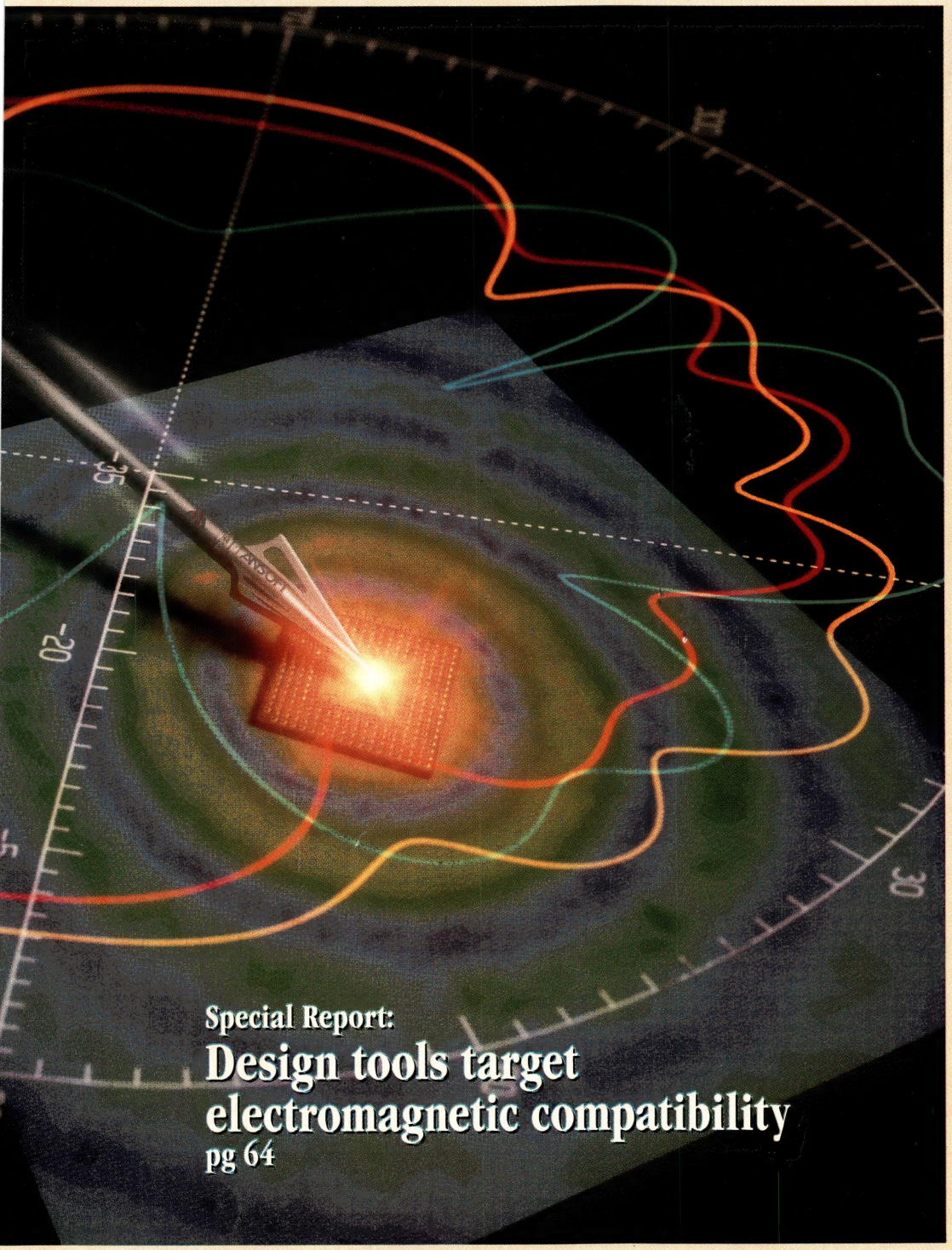
EDN®

THE DESIGN MAGAZINE OF THE ELECTRONICS INDUSTRY

February 17, 1994



Special Report:
Design tools target electromagnetic compatibility
pg 64

TECHNOLOGY UPDATES

DESIGN FEATURES

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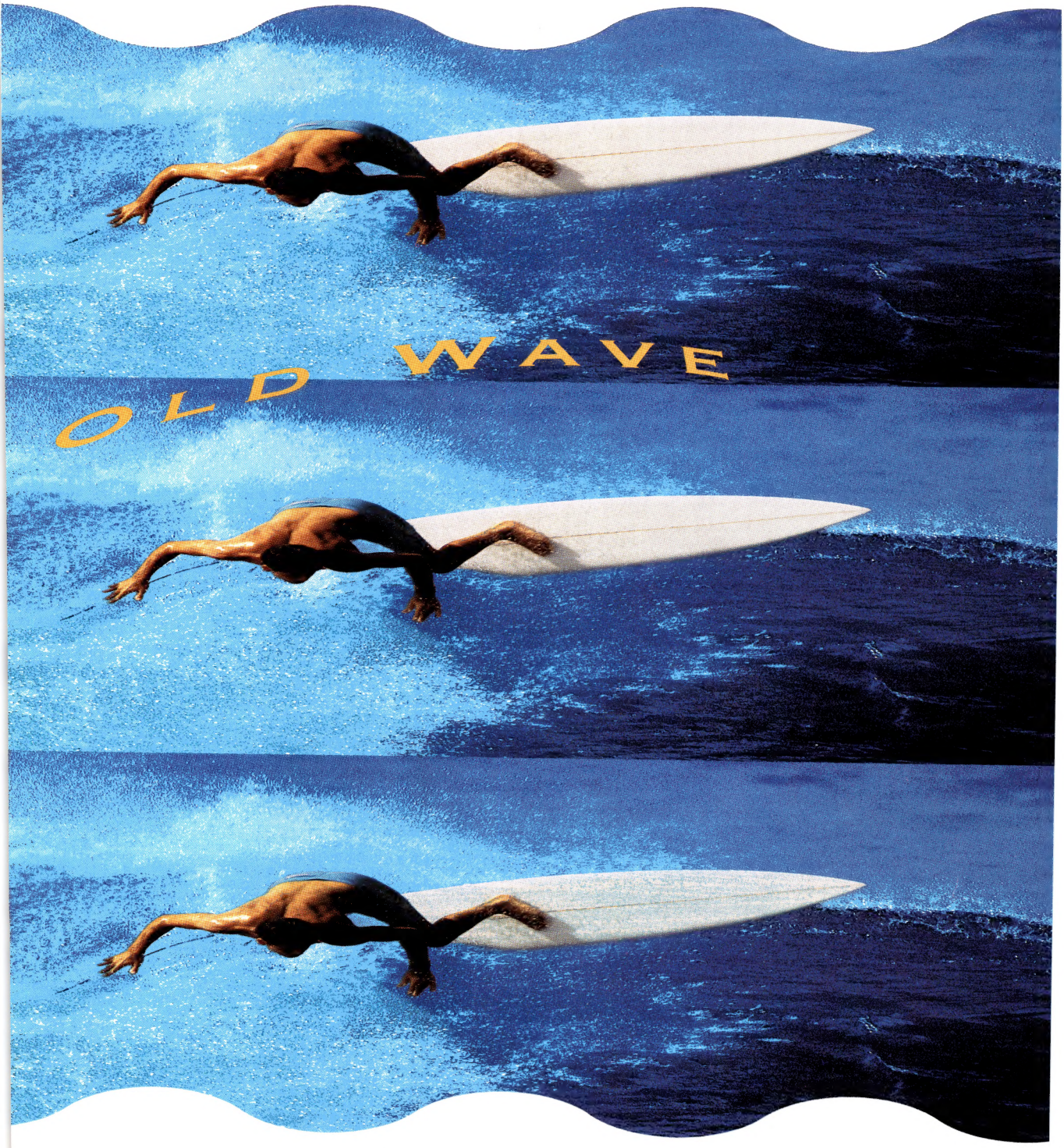

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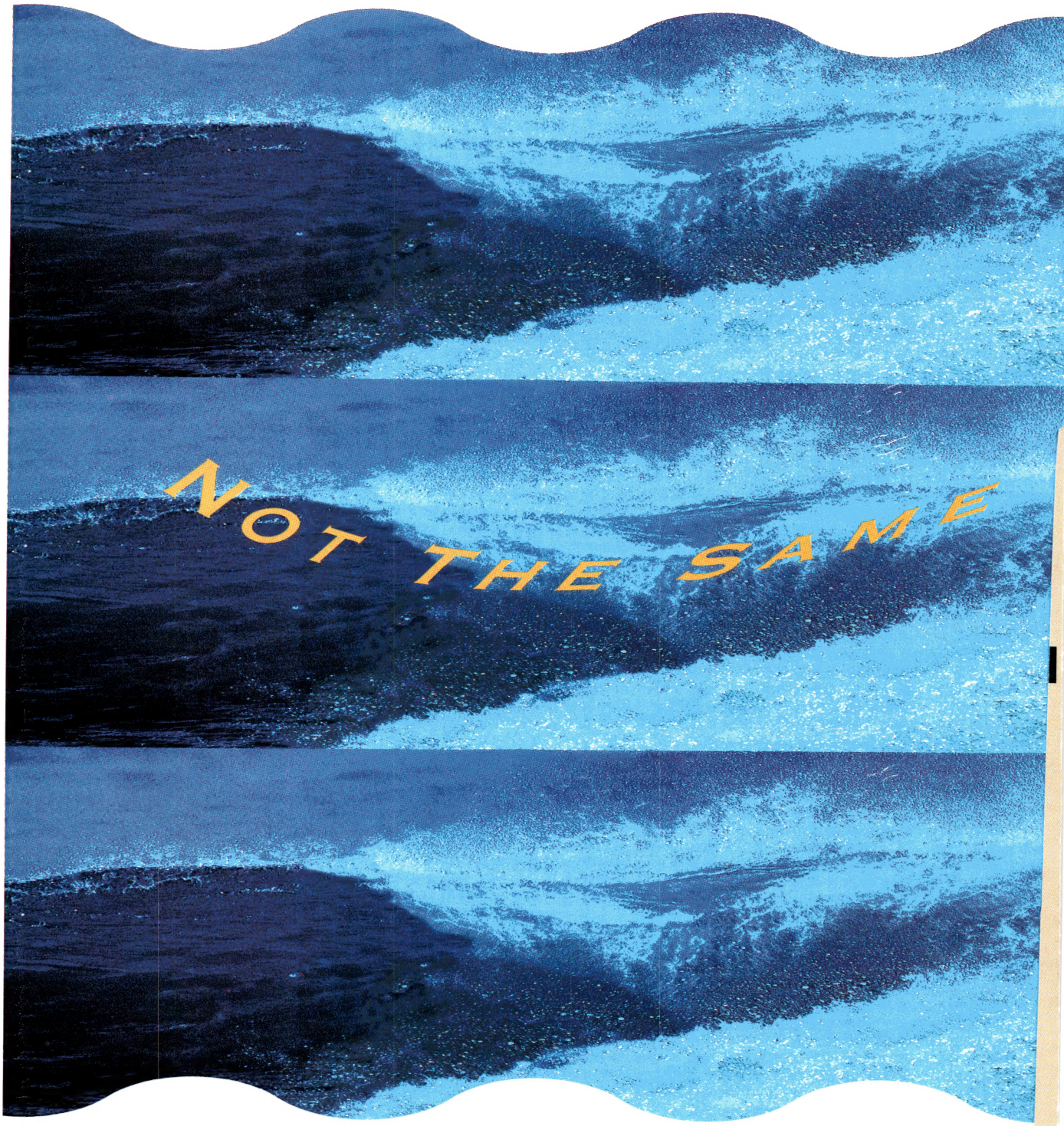

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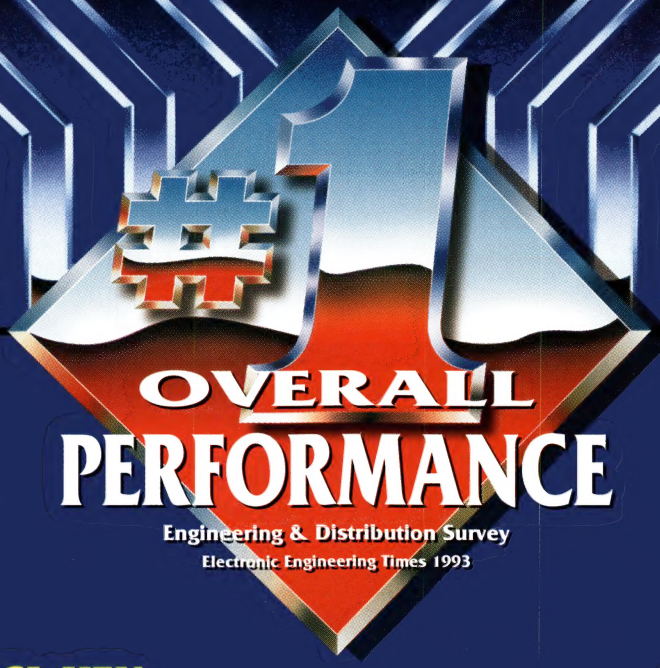

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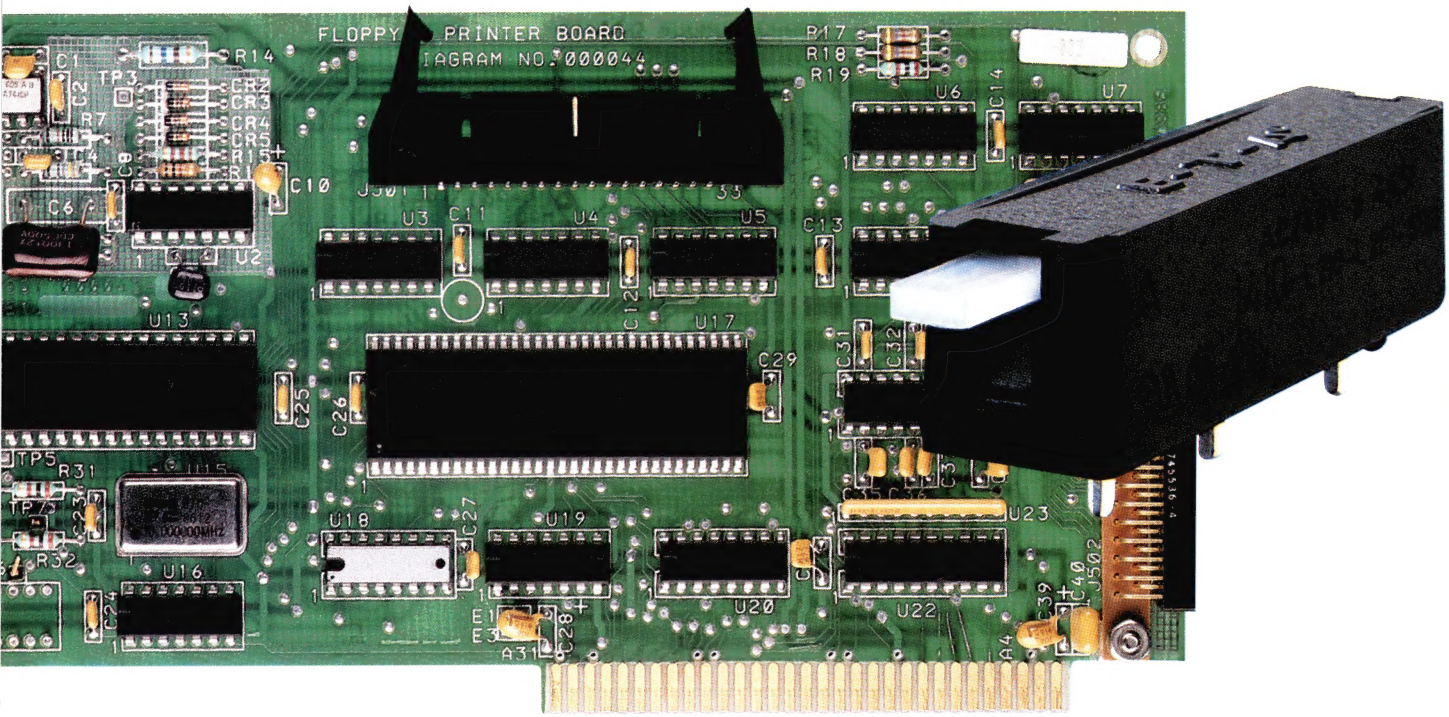

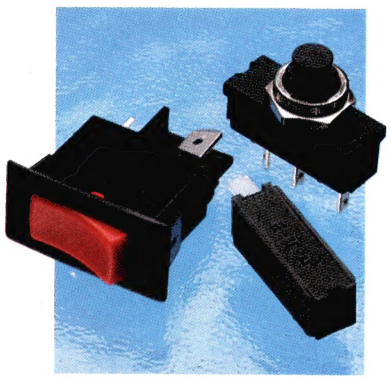

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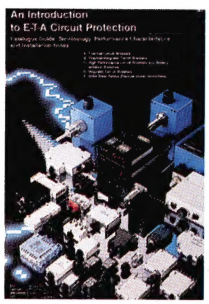

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RF Input (max dBm)	—	20	—	22	22	26
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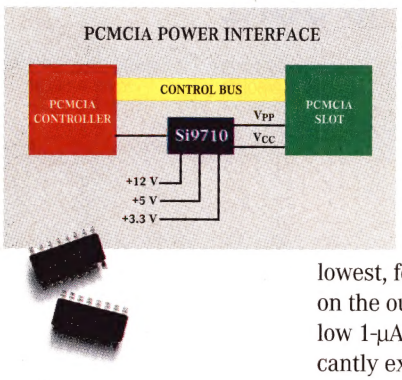

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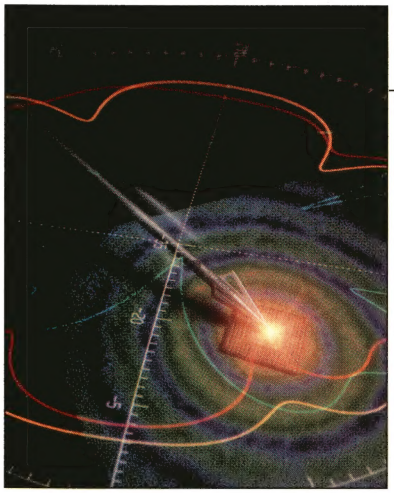

On the cover: As system speeds increase, so do electromagnetic-compatibility (EMC) problems. Several kinds of tools for EMC analysis let you address the issues early in the design game. See our Special Report, beginning on **pg 64.** (Photo courtesy Ansoft Corp; creative director, Joy Burd; art director, Rebecca Kinney; photography Caffee/Photosynthesis)

SPECIAL REPORT

DESIGN FEATURES

DESIGN IDEAS

Continued on page 7

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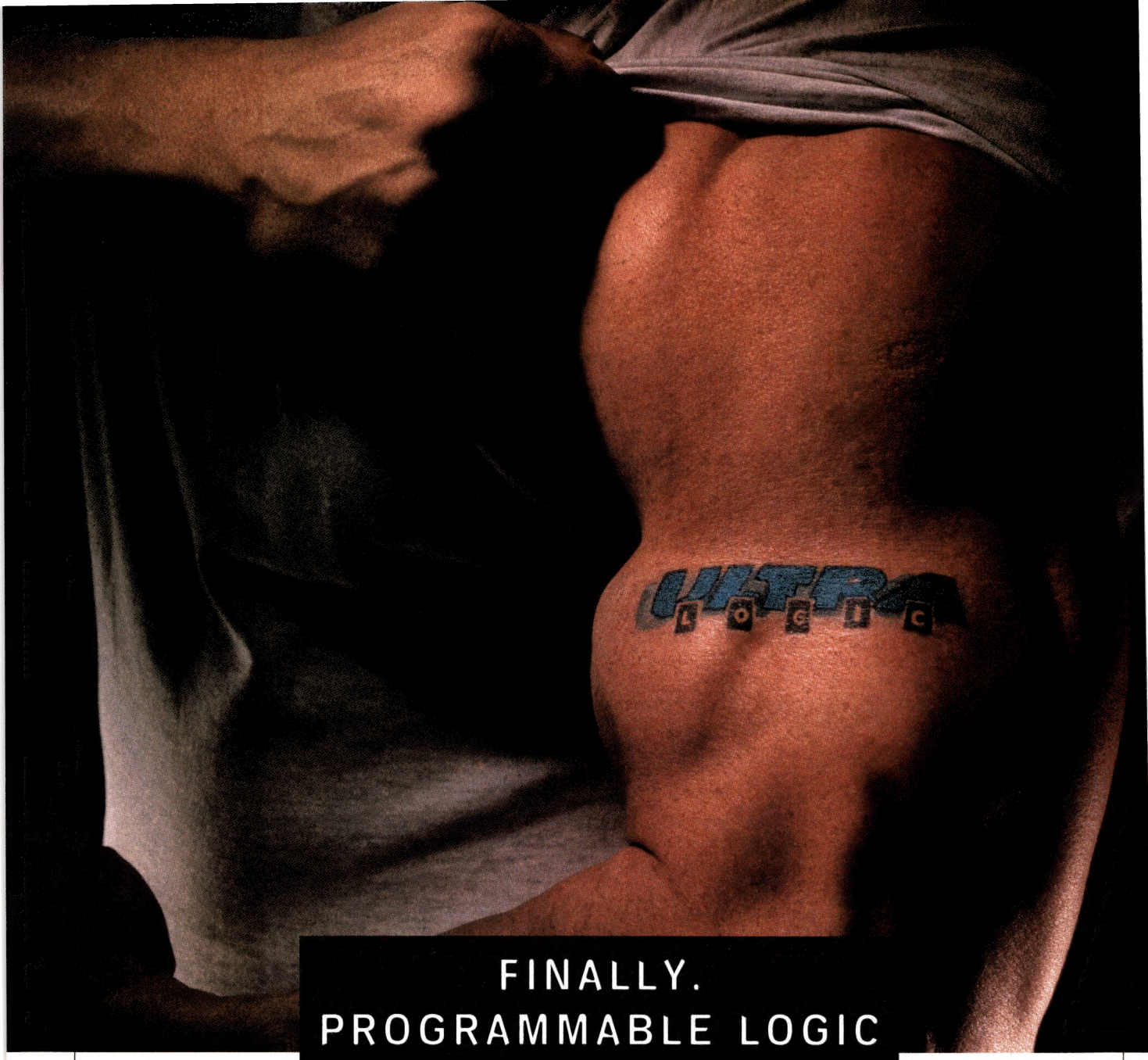

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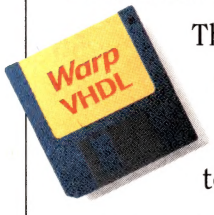

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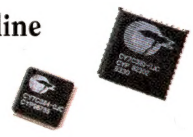

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EDN

February 17, 1994

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TECHNOLOGY UPDATES

Speech-processing ICs: Speech-synthesis and -recognition chips personalize consumer products 27

If speech is the mirror of the soul, then many of today's commercial products will reap their just rewards. Maturation of speech-compression coding algorithms is allowing almost every new device to talk, make audio sounds, and even recognize a human voice.
—John Gallant, Technical Editor

Shrinking devices put the squeeze on system packaging 41

While solving today's system-packaging puzzles, you can design products that are not only smaller but more reliable.
—Charles H Small, Senior Technical Editor

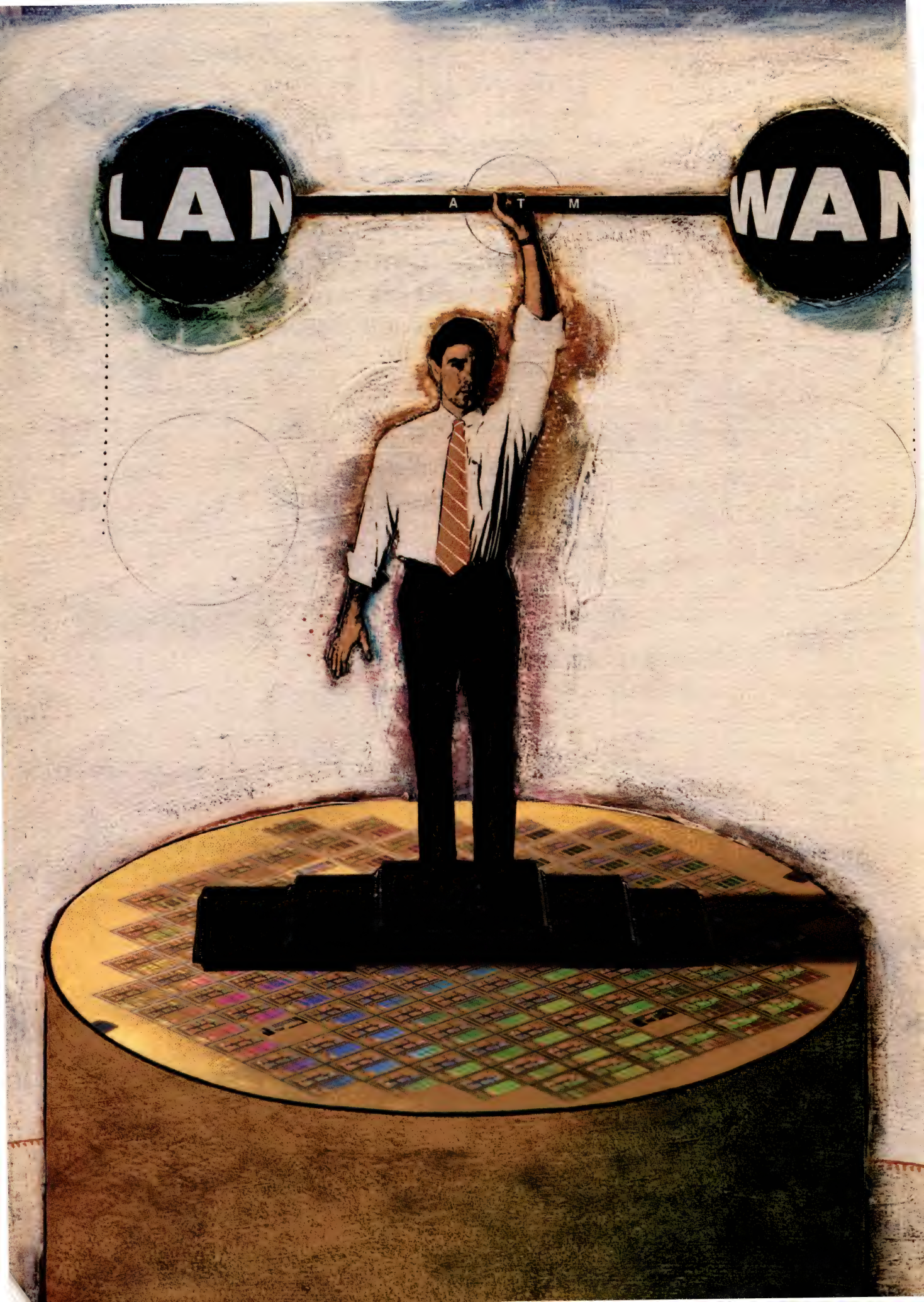
EDITORIAL

Let's get physical (again) 25

Time's up. The physics of electronics has returned to center stage, and you'd better be ready with the required tools and knowledge.
—Steven H Leibson, Editor-in-Chief

NEW PRODUCTS

DEPARTMENTS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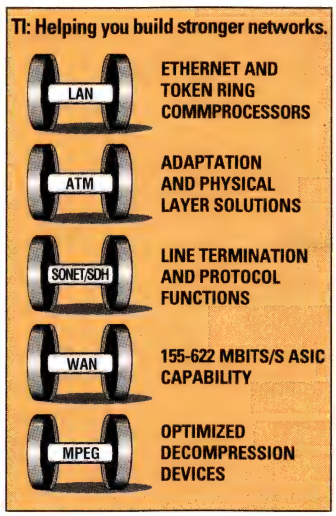

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MAX782 Output Noise Spectrum at 1A

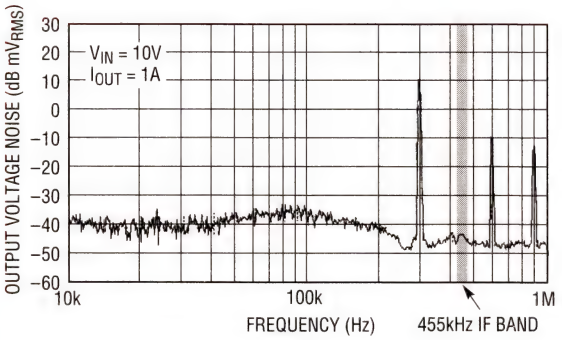

Figure 1. The MAX782 evaluation board operates at 300kHz with 1A load current and shows no harmonics in the 455kHz IF band.

MAX782 Output Noise Spectrum at 0.75A

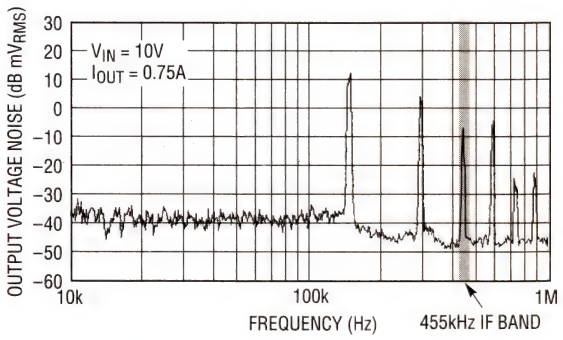

Figure 2. Dropping the load current by only 25% halves the operating frequency and shifts the third harmonic into the 455kHz IF band.

Noise in the New Generation of High Efficiency Switching Regulators.

Switching regulators generate noise. It results from the very nature of their operation, and is something that power supply designers accept to obtain the dramatic efficiency improvement compared to linear regulators. Fortunately, this noise seldom causes interference problems.

The newest battery-powered switching regulators have sophisticated algorithms which operate MOSFET switches intermittently at low load currents. Examples of these regulators are the Linear Technology LTC1148 family and Maxim Integrated Products MAX782.

While the actual algorithms differ, both can generate fundamental and harmonic frequency components over a wide spectrum.

Figure 1 and 2 above illustrate that a "snapshot" of the frequency spectrum at one load current tells the power supply designer very little. In Figure 3 the operating frequency for two different LTC1148 applications and for the MAX782 evaluation board is plotted versus load current. Figure 3 shows that the LTC1148 reaches the audio band sooner as load current falls, while the MAX782 sweeps a much wider band of frequencies while getting there. Is one better than the other? Maybe the whole issue is just a "red herring".

ED HERRING.
and switching regulators.

Lowest Noise Frequency vs Load Current

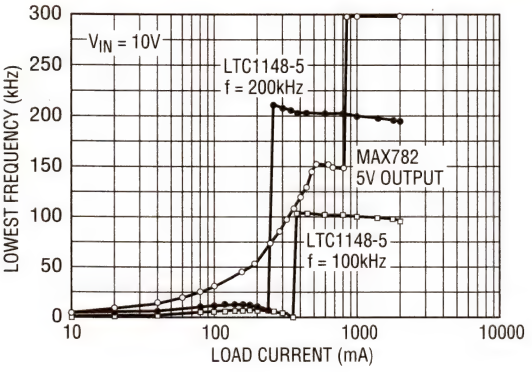

Figure 3. A more truthful look at the range of frequencies a switching regulator can generate is to plot the lowest fundamental frequency vs load current.

Noise Generated by a Notebook Computer

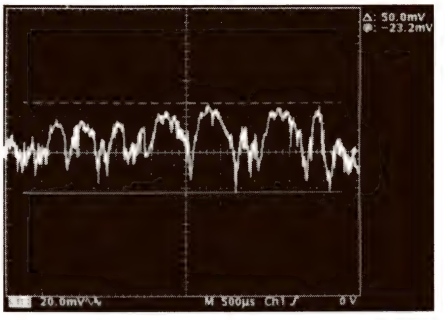

Figure 4. This photograph of a notebook computer 5V supply bus shows logic noise exceeding the ripple produced by most switching regulators.

Does Noise Equal Interference?

Switcher noise is only a *potential* source of interference, and in this regard the switcher has plenty of company. Figure 4 shows that logic noise is also rich in frequency components extending into the audio range. Fortunately, the same measures which must be taken to prevent interference due to logic noise also work on switcher output noise. These include local RC supply filters for IF and RF noise and linear regulators for audio noise.

Because all high efficiency switching regulators generate wide output noise spectra, and because it can be dealt with in the same manner as logic noise, the issue of interference is largely a red herring. Claims to the contrary by other vendors serve only to confuse power supply designers looking for the most effective solutions for their battery-powered supplies. It is other concerns such as shutdown current, quiescent current, operating efficiency, dropout voltage, transient response, and design flexibility that should rightly dominate the designer's comparison list.

For real help with switching regulators contact Linear Technology Corporation, 1630 McCarthy Blvd., Milpitas, CA 95035/408-432-1900, Ext. 361. For literature on noise in switching regulators, call **1-800-4-LINEAR.**

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CIRCLE NO. 87

EDITED BY FRAN GRANVILLE

Codecs lower cost of PC-based audio applications

Two low-cost, 16-bit stereo, CD-quality codecs provide high-performance audio for PC applications. The AD1847 and AD1846, which cost $7.50 and $8, respectively (OEM qty), both support the Microsoft Windows Sound System and Compaq Business Audio. Like the company's AD1848 SoundPort, these codecs are single-chip, sigma-delta, stereo digital-audio codecs. The AD1847's serial port allows direct interface to a DSP or system-I/O chip and fits in a low-cost 44-lead plastic leaded chip carrier or thin quad flatpack instead of the more expensive 64- and 68-pin packages parallel-port codecs require. The AD1846 is a cost-reduced, pin- and register-compatible version of the AD1848K with a dynamic range of 70 dB. Both codecs are complete digital-audio systems (including A/D conversion, D/A conversion, gain control, and mixing of multiple analog and digital data streams) and require minimal support circuitry.

—by Anne Watson Swager

Analog Devices Inc, Norwood, MA, (617) 461-3881. **Circle No. 500**

Digital-coupler IC replaces optocouplers

The ISO150 uses high-voltage capacitors instead of an LED and photodiode to transmit signals across the isolation barrier. This alternative device to high-speed optocouplers offers faster performance, lower power consumption, and better isolation specifications. The coupler also acts as a transceiver, whereas optocouplers are unidirectional. Primary applications include digital isolation for A/D and D/A conversion, multiplexed data transmission, and I/O-port isolation in instruments. The ISO150 has two bidirectional channels, which you can independently configure to transmit or receive. The IC requires no external components. Key specifications include an 80-Mbps typical data rate, 25-mW max power consumption per channel, 2400V-rms isolated partial discharge, and 16.5-mm creepage distance. The TTL- and CMOS-compatible IC comes in a 24-pin DIP and costs $7.75 (1000).

—by Anne Watson Swager

Burr-Brown Corp, Tucson, AZ, (602) 746-1111. **Circle No. 501**

Hitachi and Mitsubishi to codevelop flash memories

Hitachi Ltd and Mitsubishi Electric Corp have announced that they will codevelop flash memories. Under the agreement, the companies will jointly develop a 16-Mbit flash memory based on Mitsubishi's DINOR cell-structure technology and a 64-Mbit flash memory based on Hitachi's AND cell-structure technology. The companies will also consolidate their 16- and 64-Mbit product lines.

DINOR and AND feature higher integration and lower power consumption than NOR and NAND cell structures, which are currently the most popular technologies for flash memories. Although NOR offers 100-nsec read time and easy erasability, it requires a large cell size and a 12V external power supply. In comparison, DINOR provides a smaller cell size, single-power-source operation, and shorter access times. Hitachi's AND incorporates NAND and NOR; it also provides smaller cell size than NOR and NAND; single-power-source operation; and the ability to erase small blocks (512 bytes). AND suits nonvolatile-storage and hard-disk-drive-replacement applications; DINOR suits nonvolatile-storage applications.

The two companies expect the new technologies to become the de facto industry standard and are seeking partners with which to establish a DINOR-AND Group. One company that may join the group is SGS-Thomson Microelectronics, Europe's second-largest semiconductor company, which already has an alliance with Mitsubishi for flash-memory development.

—by Fran Granville

Hitachi America Ltd, Tarrytown, NY, (914) 333-2902. **Circle No. 502**

Mitsubishi Electronics America Inc, Sunnyvale, CA, (408) 730-5900. **Circle No. 503**

SHORTS

Correction. "News Breaks" (EDN, January 6, 1994, pg 15) provided an incorrect phone number for JTAG Technologies, the Dutch company that recently acquired Fluke Corp's boundary-scan test business. The correct information is JTAG Technologies BV, Eindhoven, The Netherlands, 31-40-785739, fax 31-40-785104. **Circle No. 504**

Rochester Electronics to offer discontinued Intel ICs. Rochester Electronics has signed an agreement with Intel Corp that lets Rochester sell discontinued Intel parts. The agreement gives Rochester access to current and future discontinued products, tooling, and processes for Intel's military and commercial ICs. Rochester Electronics Inc, Newburyport, MA, (508) 462-9332. **Circle No. 505**

Conference issues call for DSP papers. The fifth International Conference on Signal Processing Applications and Technology, scheduled for October 18 to 21, 1994, in Dallas, has issued a call for papers. Topics include DSP machines, software, and technology; instrumentation and testing; speech processing; virtual reality; and more. Abstracts are due by April 15, 1994. DSP Associates, Waltham, MA, (617) 891-6000. **Circle No. 506**

Motor uses high-temperature superconducting coils. Reliance Electric Co has demonstrated a high-efficiency motor using American Superconducting Corp's high-temperature superconducting wire. The motor offers 3730W output power, and the coils rotate at 1800 rpm, compared with the Reliance's earlier prototype, which had stationary coils and 1490W output power. Reliance Electric Co, Cleveland, OH, (216) 266-5809. **Circle No. 507**

American Superconductor Corp, Westborough, MA, (508) 836-4200. **Circle No. 508**

LITERATURE

Scope accessory catalog. This free, 16-pg, color catalog describes multimeter leads; connector adapters; and scope, differential, and active probes. **Test Probes Inc**, San Diego, CA. **Circle No. 509**

Data sheet for supplies. This color data sheet describes five single- and multiple-output supplies that produce as much as 165W. **American Reliance Inc**, Arcadia, CA. **Circle No. 510**

Signal conditioner specs. A 2-pg data sheet describes a stackable power supply that accepts charge and voltage inputs and a stackable charge amplifier that includes filters. **Scantek Inc**, Silver Spring, MD. **Circle No. 511**

Catalog lists PLL modules. A 32-page catalog lists hundreds of standard modules that collectively cover 5 MHz to 3.5 GHz. The catalog includes dimensioned outline drawings and a form for obtaining a quote on a custom unit if no standard unit meets your requirements. Free. **RF Prototype Systems,** San Diego, CA. **Circle No. 512**

Brochure covers IC test system. A 6-pg full-color brochure describes a test system for VLSI ICs that incorporate such design-for-test methodologies as I_{DDQ}, scan, and built-in self test. The system tests devices with as many as 768 pins. **Micro Component Technology Inc,** San Jose, CA. **Circle No. 513**

Catalog on interconnect products. A 260-pg catalog describes more than 10,000 products, including accessories for in-circuit emulators, programmers, and logic analyzers. Free. **EDI Corp,** Patterson, CA. **Circle No. 514**

Guide describes bioelectric measurements. The Axon Guide covers topics in neuroscience, cardiovascular research, and plant physiology research. It covers such subjects as data acquisition and how to minimize noise in laboratory setups. **Axon Instruments Inc**, Foster City, CA. **Circle No. 515**

Book lists industrial I/O products. This 96-pg free catalog describes such items as ADC boards and arbitrary-waveform generators. Industrial Computer Source, San Diego, CA. **Circle No. 516**

Tutorial on scope probes. This 36-pg illustrated booklet explains probing basics and how to select scope probes. It also contains a glossary. Free. **Tektronix Inc,** Beaverton, OR. **Circle No. 517**

Intergraph ships Windows NT-based design system

Intergraph Corp, the largest independent application site for Microsoft's Windows NT operating system, is now shipping the VeriBest Design System for Windows NT. The software provides an integrated system comprising a schematic editor, a state-diagram editor, an online electrical-rules checker, an automatic Verilog or VHSIC hardware-description-language generator, a Verilog simulator, and a graphical logic analyzer. The complete VeriBest Design System software costs $22,000. Unbundled design software costs from $3500.—by Doug Conner

Intergraph Corp, Huntsville, AL, (800) 837-4237. **Circle No. 518**

IEEE 802.12 accepts HP draft spec

Hewlett-Packard Co has announced that the IEEE 802.12 working group voted to accept HP's Demand Priority protocol (100VG-AnyLAN) draft specification, which HP submitted at the IEEE 802.12 interim meeting on January 17 to 19 in Austin. The specification includes Token Ring additions IBM, Proteon, and Texas Instruments proposed.

HP believes this brings the IEEE 802.12 working group one step closer to final approval of a draft standard for transmitting Ethernet and Token Ring information at 100 Mbps. To ensure Ethernet and Token Ring frame compatibility, the IEEE 802.3 (Ethernet) and IEEE 802.5 (Token Ring) committees each have assigned two voting liaisons to the IEEE 802.12 working group.

HP's 100VG-AnyLAN provides users with standard, compatible, and affordable 100-Mbps performance to desktops using Ethernet or Token Ring frames. The Demand Priority protocol supports all of the network design rules, topologies, and cable types of 10Base-T and Token Ring, and it gives users an easy and economical upgrade to higher performance.

—by Fran Granville

Hewlett-Packard Co, Palo Alto, CA, (415) 857-1501. **Circle No. 519**

ATM network-interface card runs on PCs

In response to increasing demand for Asynchronous Transfer Mode (ATM) communications, Newbridge Microsystems has expanded its Openbus Communications product line by introducing an ATM network-interface card for standard EISA-based PCs.

The NM 121 ATM adapter operates on PCs running Novell NetWare, NetWare Lite, Microsoft MS-DOS, and Microsoft Windows. It also complies with NetWare servers and PC clients. The NM 121 ATM adapter supports up to 100-Mbps throughput over multimode fiber; it complies with ATM Forum specifications; it provides comprehensive remote management using SNMP; and it accomodates industry-standard protocols including IPX and TCP/IP.—by Fran Granville

Newbridge Communications, Ottawa, ON, Canada, (613) 591-3600. **Circle No. 520**

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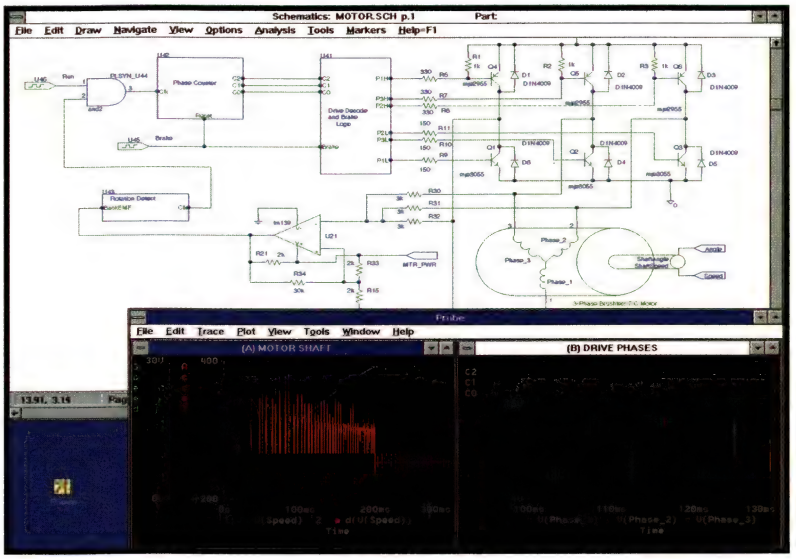

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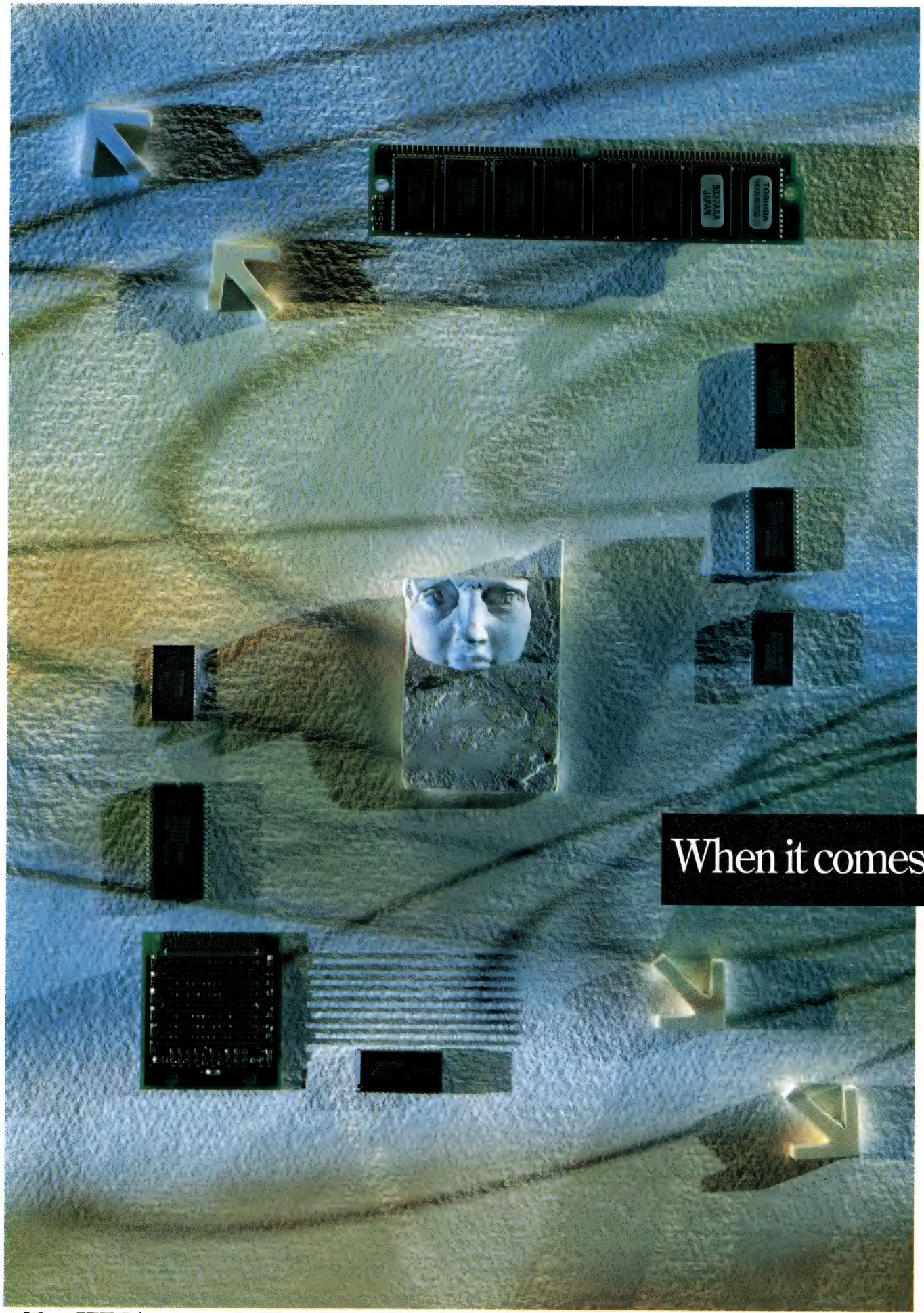
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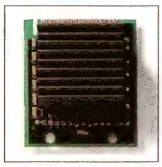
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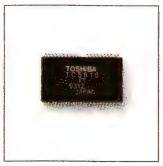
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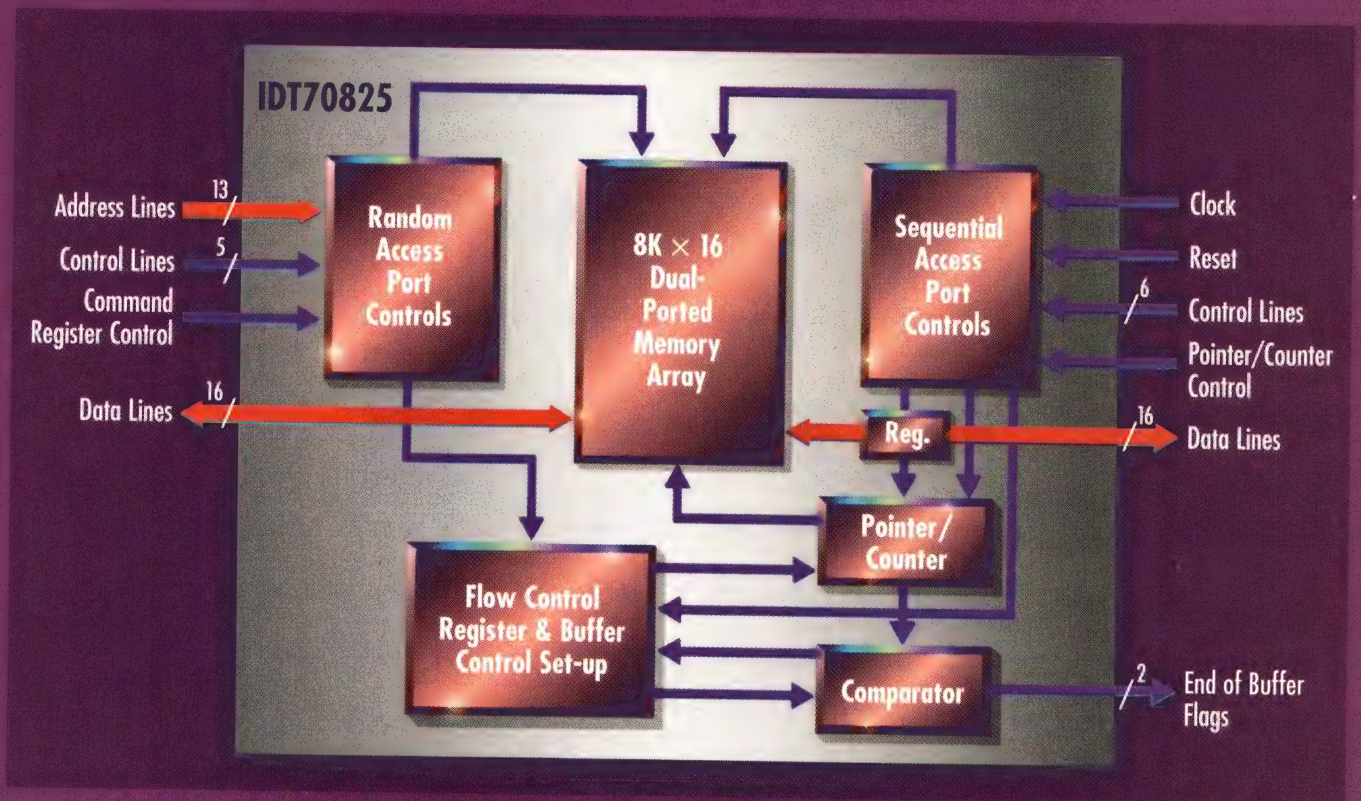

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Correct the spec

In the new-product writeup for the LT1413 dual single-supply op amp (*EDN*, November 11, 1993, pg 122), you describe the op amp as having a maximum supply current of 480 mA/amplifier; in fact, the supply current is 1000 times lower than that: 480 μA/amplifier. Its drift is 0.5 μV/°C, rather than 0.5 μC/°C. Please alert your readers.

Ron Denchfield, Public Relations
Linear Technology Corp
Milpitas, CA

Equation corrections

Thank you for publishing my article, "Relative-phase modeling speeds Spice simulation of modulated systems" (*EDN*, November 11, 1993, pg 91). Unfortunately, several errors appeared in the equations; the inconsistent math may confuse readers.

- In **Fig 1b** (pg 92), the signal coming from the left-most summer should be labeled Φ_I
- **Eq 2** (pg 93) should read $v_0(t)=\sin(\Theta_C(t)+\Theta_D(t))=\sin(\omega_C t+\Theta_D(t))$
- The equation just below **Eq 2** (pg 93) needs an = just after $\Theta_D(t)$
- Near the end of the first paragraph on pg 94, f_I should be Φ_I
- Also on pg 94, in the lower right corner, the first three of the four equations were typeset as ω@-1t but should have read $\omega_I t$; the fourth of these equations should have a) just before the =
- Finally, in **Fig 3** (pg 94), the last signal's label should be ϕ_I.

John Kesterson, Sr Engineer
Mitsubishi R&D Center
Nevada City, CA

Innovation is thriving

I cannot resist commenting on your editorial "Innovation is where you find it" (*EDN*, November 25, 1993, pg 33). It seems to me that you are making a "left-brain" analysis of your friend's "right-brain" comment. Is innovation dead? Of course not. We in the United States are as innovative as any group on earth. One serious problem, however, is that our business and political philosophy is not tuned to searching out and rewarding innovative ideas. Perhaps you have noticed, however, that the Japanese do just that.

And now for a specific suggestion: Because so few technical magazines pay much attention to patents, how about publishing a 1-pg feature on electrical patents granted? For example, you might try a review of a publication such as "NASA Tech Briefs."

Wayne E Hough
President, Kryptos Corp
Mukilteo, WA

Motorola photo lacks text

At the bottom of pg 24 of our "Have a high-tech holiday" feature (*EDN*, December 9, 1993), we ran a photo of a Motorola evaluation board but printed the wrong product writeup under it. Motorola's hands-on kit includes the fully assembled bar-graph pressure-gauge evaluation board, an application note, a sensor brochure, two data sheets, a sensor slide rule, and a sensor pocket conversion card. You need only apply pressure to the MPX2100 pressure sensor to interface with digital systems. The kit costs $75. Phone (800) 441-2447 and ask for KITDEVB147/D.

Experiment with floor planning

Regarding Doug Conner's Technology Update "ASIC design tools: Submicron technologies require floor planning" (*EDN*, September 2, 1993, pg 61), I would like to share some experience with floor planning vs flat placement and wiring.

We designed several CMOS processors and I/O chips in an IBM 0.8-μm CMOS technology and compared these designs using a flat-vs-floor-planned approach. The following specs show the complexity of a typical design:

- 12.7-mm chip size
- 343,200 available GA/SC cells
- 330,836 (96%) used GA/SC cells
- 13 macros
- 34,935 used circuits
- 3200k transistors.

I agree that flat layout without a timing-driven approach is likely to result in a poor cycle time, but we've seen that in the case of a timing-driven place and route, the flat version is superior to the floor-planned version. (Timing driven in this case means that we automatically generate upper bounds for the wiring length of each net and use this information to drive the placement and wiring.)

To show the strength of this

Table 1—Postlayout timing analysis
(cycle time with zero wiring set to 100)

Cycle time	Number nets with negative slack	Floor plan	Timing-driven place and route
129	3556	No	No
113	2096	Yes	No
114	889	Yes	Yes
109	571	No	Yes

approach, we calculated the possible cycle time with zero wiring length for each net; we used only the capacitance of the inputs of the next stage driven by the net as the actual net capacitance. This yields a theoretical lower bound for the possible cycle time. For this example, we've set this lower bound to 100 and used this as (an unreachable) target for layout.

The results (see **Table 1**) show the possible cycle times for each of the four possible combinations of flat/floor-planned and timing driven/nontiming driven. Column 1 shows the number of nets that do not satisfy the timing requirements; reducing this number makes the job of incremental logic change (to improve cycle time) much easier.

"Submicron technologies require floor planning" is true for the nontiming-driven approach, but for the timing-driven approach, the flat version is superior. In this case, the actual cycle time is only 9% above the theoretical lower bound of wiring length zero.

We obtained similar results for several test cases and are now using flat, but timing-driven, layout for all of our production chips. Due to very fast place-and-route algorithms, the turnaround time is two to three days.

This is not to say that some type of early floor planning and feedback of the estimated net length to synthesis isn't useful, but even in this case, I suppose that not using the floor-plan boundaries in the final place and route improves timing. Probably, a combination of both approaches is preferable.

Dr Jürgen Koehl
IBM Deutschland Entwicklung GmbH
Böblingen, Germany

Review of "Hands On!"

I am a very satisfied user of Byte Craft's Fuzz-C preprocessor, which you covered recently in your "Hands On!" column (*EDN*, December 9, 1993, pg 223). Most recently, I used it in an embedded controller based on a Motorola 68HC11 and was pleased with both the performance and code size of the fuzzy-logic functions. I am currently using a beta version of the preprocessor, which incorporates some of the upcoming improvements—specifically the use of variables in LINGUISTIC and CONSEQUENCE blocks. I feel strongly that tools, such as Fuzz-C, that generate standard C code have much greater utility than those that produce assembly language for one (family of) microprocessor.

I am puzzled by David Brubaker's comments toward the end of the review. He suggests an improvement to Fuzz-C would be "...a Windows icon with which a user could open and execute Fuzz-C." Most Windows users know how to create an icon or a PIF file to run a DOS application from Windows. The process is relatively simple and takes just a few minutes. I am really amazed, however, by the statement that the author "had to...temporarily exit Windows, run Fuzz-C under DOS, and then reenter Windows to compile and debug." Even a novice should be able to open a DOS window and run Fuzz-C *without* leaving Windows!

Overall, the review was thorough and accurate, and I encourage *EDN* to present more articles and reviews of embedded-systems development tools.

Eric B Schuyler
EBS Consulting
Snyder, NY

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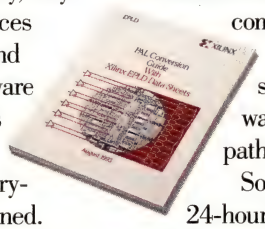

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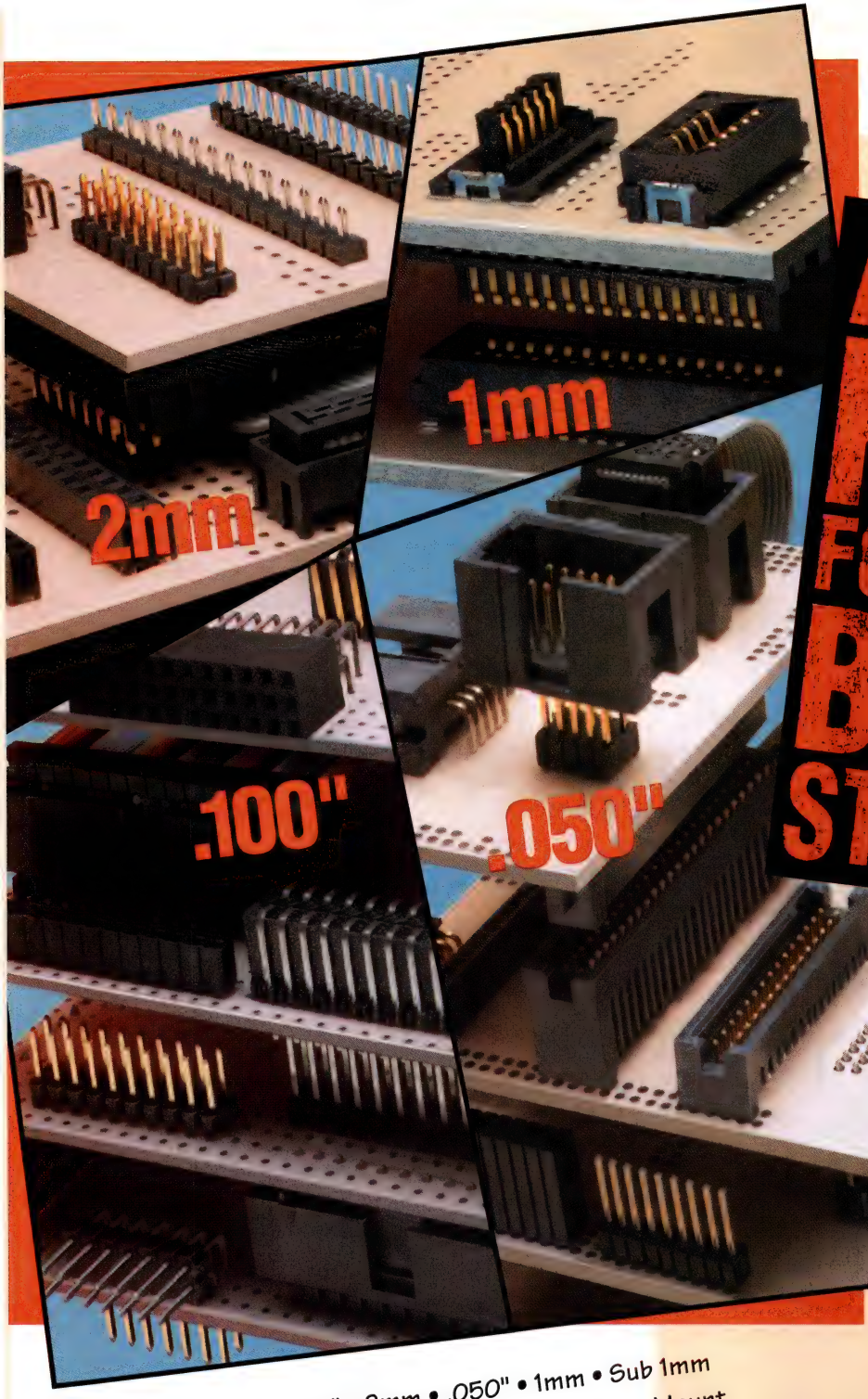

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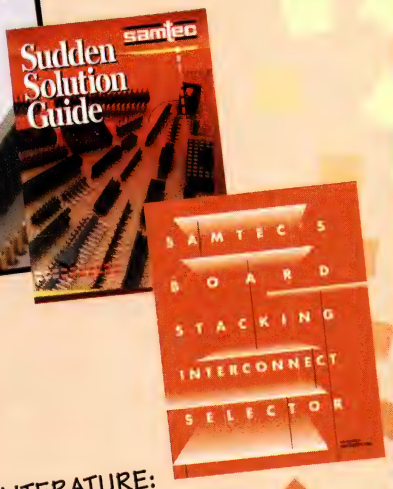

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CIRCLE NO. 80

Let's get physical (again)

In the days before the world went digital, electrical engineers dealt with physical reality. In fact, their design prowess depended heavily on their ability to subjugate various physical laws armed with little more than a slide rule and a book of engineering formulas. Then came RTL, DTL, HTL, SUHL, ECL, TTL, CMOS, and a host of other abbreviations all translating to one word: digital. Digital electronics threw a lot of physical reality out the window.

For example, in the TTL domain, 2 and 5V mean the same thing. Ditto 0 and 0.5V. Face it; things were sloppy in the digital realm, and we loved it. Recently, Isadore Katz of Meta-Software came by to tell me something that I already knew: The party's over. Physics has returned to electronics. Speeds have increased, and geometries have shrunk to the point where parasitics now have a substantial effect on digital circuit operation.

Katz specifically talked about circuits in deep submicron ICs, but the same is true at the board level. You can't build leading-edge, 0.35-μm ICs without seriously sparring with physics, and you can't plop a 200-MHz μP with its support circuitry onto a pc board without a similar analysis. If you want to compete in today's market, you're sooner or later going to have to work with deep submicron ICs and high-speed pc boards.

In the micron realm, IC designers have been simulating circuit performance for many years. However, to save time, IC circuit simulation has generally coupled linear or piecewise-linear approximations with lumped parasitic elements. Not any more. At 0.35 μm, approximations won't get you close to the theoretical maximum clock speeds of the silicon. To really exploit advanced IC-fab processes, you've got to get physical, and that means simulating the real circuit phenomena. Likewise, the era of pc-board design using Kentucky windage has ended; parasitics rule. Wide 64-bit, 200-MHz μP buses present just as many pitfalls as deep submicron ICs.

While Katz's mission was to point out how important his company's HSpice simulator will become for deep submicron IC design, his message really has a much broader scope. No matter which type of design you're doing, if you want to compete, you'd better dust off your physics and sharpen your simulation skills. This time around, however, you're better off leaving the slide rule in its glass display case.

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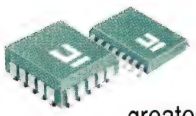

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SPEECH-PROCESSING ICs

Speech-synthesis and -recognition chips personalize consumer products

JOHN GALLANT, Technical Editor

If speech is the mirror of the soul, then many of today's commercial products will reap their just rewards. Maturation of speech-compression coding algorithms is allowing almost every new device to talk, make audio sounds, and even recognize a human voice.

Have you ever noticed how virtually every consumer product you buy these days can talk to you? Practically every new toy, learning aid, game, and even some greeting cards can make audible sounds. In addition, multimedia computers, automotive warning systems, appliances, clocks, and equipment for the handicapped all can talk. At the core of these talking devices are speech-synthesis ICs that generate speech from sampled data stored in memory.

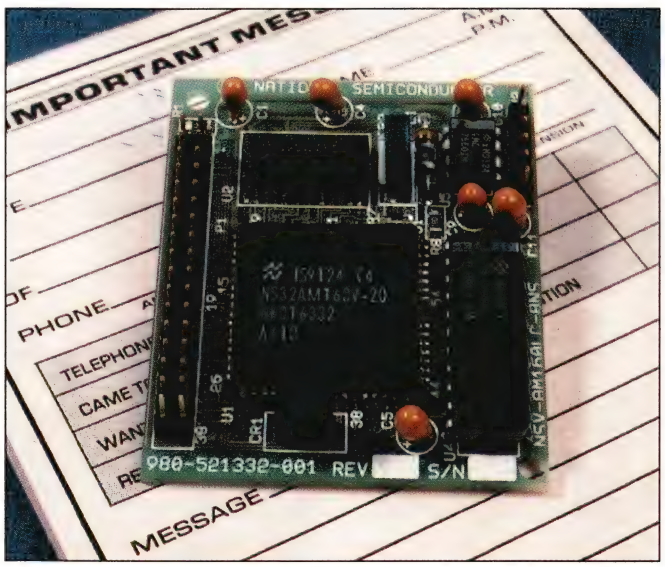
The 1980s witnessed a range of technical breakthroughs that enable today's high-quality talking products. Gone are the early days of talking computers, which employed ICs that linked phonemes to generate speech. Although these products could generate unlimited speech, the speech was of very poor quality: At best, it sounded robotic; at worst, it was unintelligible. The techniques that emerged to generate today's high-quality speech are sampled-data systems that take samples of an actual human voice. The systems use data compression for predictive-coding algorithms.

The two most popular predictive-coding algorithms for generating speech are adaptive differential pulse-code modulation (ADPCM) and linear predictive coding (LPC). These algorithms compress speech samples stored in memory while retaining "near-toll-quality" speech. The CCITT defines toll-quality speech as logarithmic PCM-coded data at a sample rate of 8 kHz and a resolution of 8 bits/sample. The combination results in a bit rate of 64 kbps for toll-quality speech.

ADPCM has lots of advocates

Oki Semiconductor uses the ADPCM coding system to compress data in the company's speech-synthesis ICs. ADPCM is a variant of DPCM, which reduces the amount of data by quantizing and encoding the differential between speech-signal samples. ADPCM adaptively changes the quantization width, depending on the quantization width of the previous differential sample.

Oki offers synthesizers having internal mask ROM ranging from 128 kbits to 1 Mbit. The company also offers synthesizers with one-time-programmable (OTP) or external ROMs, (**Fig 1**). The synthesizers have resolutions of 3 or 4 bits/sample and variable



Cassette answering machines are giving way to digital tapeless answering machines, such as this one from National Semiconductor. The NS32AM160 contains DSP functions, 25 kbytes of ROM, a codec, and 2.1 kbytes of RAM to implement the voice-handling algorithms.

SPEECH-PROCESSING ICs

sampling rates from 4 to 16 kHz. A 4-bit ADPCM synthesizer sampling at 4 kHz has a compressed bit rate of 16 kbps. The 4-bit MSM6379 has 512 kbits of OTPROM, which stores 32 sec of speech sampling at 4 kHz. The $10 (5000) chip comes in a 16-pin DIP and has an internal 12-bit D/A converter and a lowpass filter. You program the device using a dedicated programming tool called Anawriter Mark VII.

Mosel-Vitelic also offers a wide range of speech-processing chips, largely designed into products from Asia, based on ADPCM data compression. The VTV001 has as much as 256 kbytes of memory and variable bit rates from 16 to 32 kbps. The chip also includes a microphone and a preamplifier for voice recording and an 8-bit D/A converter for reproduction.

Looking ahead

Speech-synthesis technology has matured through the 1980s and the 1990s. As a consequence, you can purchase powerful speech-synthesis ICs today for only a few dollars or less in OEM quantities. The low added cost of these devices must appeal to commercial-equipment designers because they are including vocal commands in virtually every product under development.

Even speech-recognition technology has made major advances in the past decade. Although the most sophisticated voice recognizers require a computer with megabytes of memory, voice-recognition products designed around DSP chips or embedded processors are powerful subsets of this technology. These speaker-trained devices store a variety of utterances and achieve accuracies greater than 90%, even in the presence of automobile noise. You can expect to see these products in cellular and cordless telephones, handheld personal digital assistants, digital answering machines, and a variety of voice organizers, such as memos, calendars, and to-do lists.

LPC models the vocal tract

Texas Instruments employs the other popular coding system, LPC, to compress data in speech-synthesis ICs. LPC attempts to model the human vocal tract. Air from the lungs excites the vocal tract by moving through the vocal chords (two small flaps at the base of the larynx). When producing voiced sounds such as "a" or "e," the vocal chords vibrate to modulate the air from the lungs, thus producing nearly periodic pulses of air. The pitch period determines the sound produced.

Besides the voiced sounds, generating speech also requires the use of unvoiced—or noise—sounds, such as "s." Turbulent air passing through the open vocal tract produces unvoiced sounds. Above the vocal chords are the pharynx and the oral and nasal cavities, all of which shape the spectrum of the sound. The frequency response of the vocal tract is similar to a tube with constant diameter, which has a number of resonances, or formants.

TI's TSP50C1x family combines an 8-bit μP, a speech synthesizer, ROM, RAM, a D/A converter, and I/O interface ports on a low-cost chip. The chip's LPC model imitates the human vocal tract. The model extracts parameters from sampled speech to create two excitation generators that model the vocal-chord restrictions for voiced and unvoiced sounds. The model has a gain multiplication stage to model levels of pressure from the lungs and a 12-pole lattice filter that models the shape of the oral cavity. Because the filter has 12 poles, TI calls it LPC-12 (**Fig 2**).

Because speech changes slowly, the μP accesses parameter samples from memory in frames that are generally 10 to 25 msec long. The device calculates the input parameters to the model as an average of the parameters for the entire frame. The resulting compressed bit rate is effectively 1.5 kbps. The TI devices offer five sizes of internal ROM ranging from 4 kbytes (capable of processing 14 sec of speech) in the $0.85 TSP50C04 to 32 kbytes (capable of up to 3 minutes) in the $2.30 TSP50C19. Because the devices are mask programmable, they are available only in minimum-quantity orders of 50,000 units.

TI recommends that external speech-coding services perform speech development for the company's speech-synthesis chips. One external speech developer is Robert Jeffway, who has coded a host of toys and commercial appliances using TI's development tools for speech analysis. You can contact him in Leeds, MA, at (413) 584-0491.

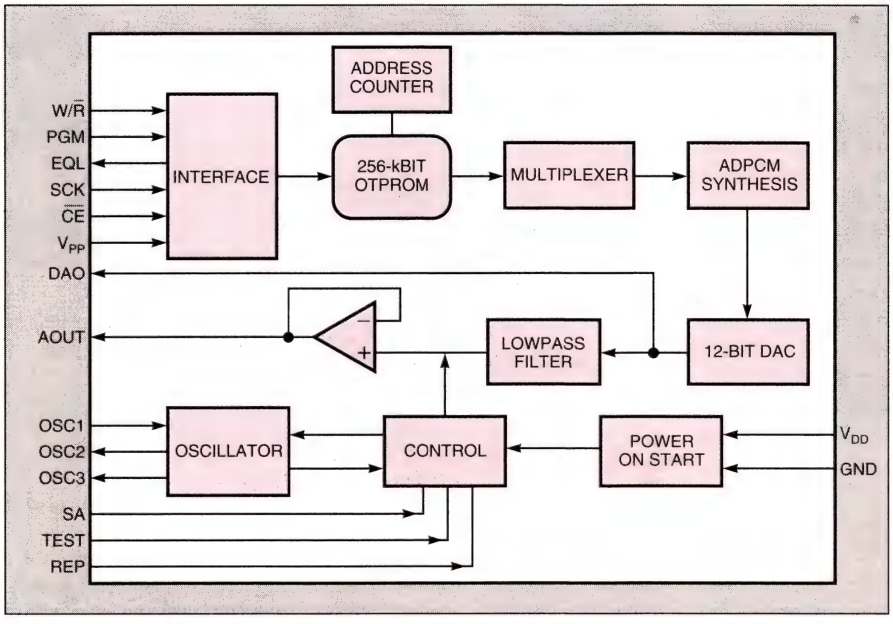


Fig 1—The MSM6378A chip from Oki Semiconductor is an ADPCM voice synthesizer having 256 kbits of OTPROM. At a 4-kHz sampling rate, the chip stores as much as 16 sec of speech.

Toys and games

ESS Technology offers the Sound Magician line of speech- and sound-synthesis chips for the toys and game market. The playback-only chips cost $0.50 to $2 in OEM quantities. A customer

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supplies a recording of the desired speech and sound, which the company samples and stores in an on-chip ROM.

In addition, ESS supplies three chips that generate speech and sound for PC applications. The chips employ ADPCM or a patented ESPCM compression coding algorithm. The chips are register compatible with Creative Labs' Sound Blaster board. The $12 ES488 creates all of the speech and sound of a Sound Blaster board, except music synthesis.

The recently introduced $18 ES1488 is socket compatible with the ES488 and includes on-chip music synthesis. The $20 ES688 is a 16-bit stereo chip that features 44.1-kHz sampling for recording and playback of CD-quality music. All of the chips interface with the ISA bus and have drivers for Windows and the Windows Sound System. The chips' audio-application software includes an audio recorder, a talking clock, a calculator, and a volume control. In addition, the chips run on 3.3 or 5V and have power-management features for adding sound to portable computers.

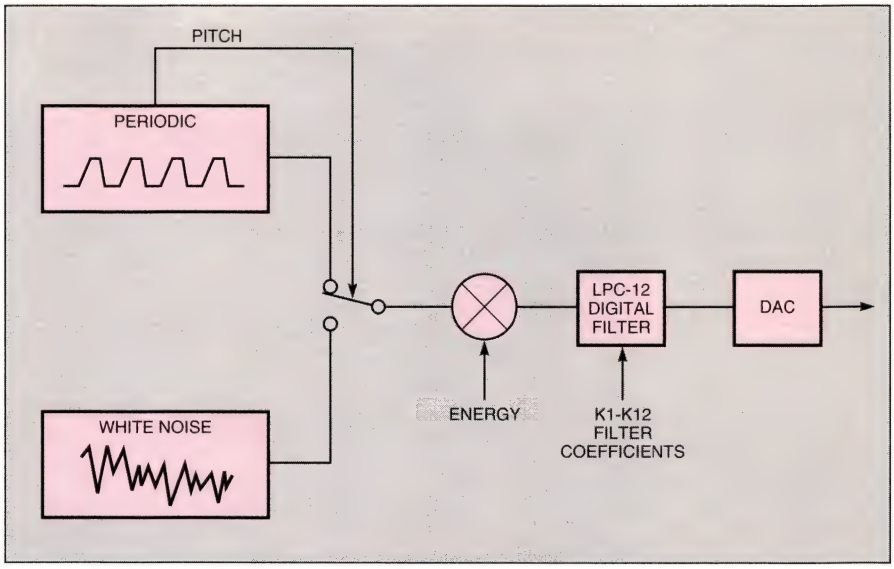

Fig 2—TI's TSP50C1x family of LPC voice synthesizers model the human vocal tract. Two generators for voiced and unvoiced sounds drive a digital filter, which models the human oral cavity.

National Semiconductor's NS32AM160 and NS32AM161 chips are members of the 32-bit Series 32000/EP family of embedded system processors. Designed for digital answering machines, the $18 (10,000) chips can also replace microcassettes in dictation machines. The processors integrate the functions of a DSP chip and a system controller. The DSP function compresses and decompresses data using sub-band coding or LPC algorithms.

The processors can execute instructions from on-chip or external ROM. In addition, the chips can detect and generate DTMF tones and provide voice recognition. National supplies the NSvoice algorithmic software to execute the DSP, compression/decompression, DTMF, and tone-generation functions.

Information Storage Devices (ISD) provides a different twist to recording and playback devices for short (10 sec or less) speech applications. The $5.48 (1000) ISD1100 series stores analog signals directly in single cells as one of 256 levels. Each device provides an oscillator, a microphone preamplifier, automatic gain control, a smoothing filter, and a speaker amplifier on one chip.

Because the ISD chips provide analog storage, they don't require A/D or D/A converters. ChipCoder technology lets you record and rerecord as much as 10 sec of audio without using a special programmer. You can play back the sound through a small external speak-

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SPEECH-PROCESSING ICs

er. The chip is at the heart of Hallmark's recordable greeting cards.

Voice synthesis is only half the story. Many commercial devices can recognize voice commands as well. Because voice-recognition algorithms are more complex than synthesis algorithms, they require the full horsepower of a DSP chip. AT&T has leveraged its expertise based on the DSP16A chip to develop dedicated speaker-trained voice recognizers for telecommunication terminals, such as cellular and cordless telephones. Using ADPCM or code-excited linear-predictive-plus coding, the recognizers store compressed speech that achieves bit rates of 5.2 kbps.

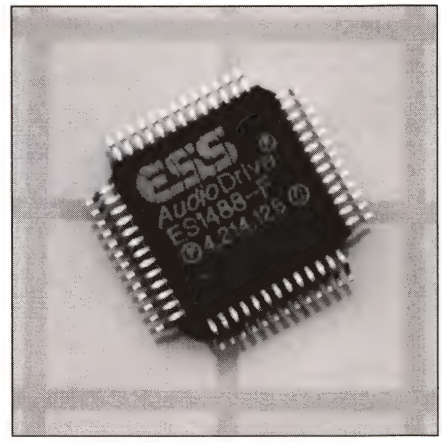
AT&T's latest offering is a hands-free voice processor, called the HVP-S, which provides full-duplex operation of a cellular phone with no microphone suppression. The chip, along with two codecs, memory, and a microcontroller stores as many as 64 speaker-trained utterances. The chip allows speed dialing by voice and automatically answers the phone. The HVP-S with ROM-coded voice-recognizer software sells for less than $20 (10,000).

Because Analog Devices sells some of its DSP chips for less than $10, the company is actively recruiting third-party vendors to add speech-processing value to their chips. For example, Centigram Communication adds interactive voice response and text-to-speech value to its 2100 family of DSP chips. You can purchase the product as an adapter card or as integrated chip sets.

Recently, Dragon Systems and Analog Devices received a federal grant to port Dragon's voice-recognition software onto one of Analog Devices' DSP chips. Dragon will develop speech-recognition software to fit available memory and run on a range of DSP chips for handheld personal digital assistants and notebook computers.

Voice recognition for faxes

National Semiconductor offers the Dispatch family, which includes three 32-bit embedded processors that incorporate DSP functions and three peripheral controllers. The product permits the use of a single phone line for facsimile and voice communications. It uses software to switch automatically between send and receive modes or between voice and fax modes. Dispatch uses a set of 25 words to provide speaker-dependent voice recognition for controlling the fax and the answering machine. The lowest configuration of the family—the 32FX161 processor plus the 32X100 peripheral controller—costs $45 (1000).



ESS Technology's ES1488 IC is a complete Creative Labs Sound Blaster board on a single chip. The chip runs on 3.3 or 5V and offers power-management features.

Vocal Inc adds voice-recognition software to TI's TMS320C25 DSP chip or National Semiconductor's 32000/EP family of embedded-system processors. The company's TrueWord software stores as many as 100 utterances using a speaker-trained DSP algorithm called Spectral Fit Coding (SFC). SFC compresses sampled audio data to 5 kbps using a minimum-squared error-fitting process.

For systems that already have a TI DSP chip or one of National's embedded processors, Vocal supplies TrueWord as a licensed OEM software product. Otherwise, Vocal offers a 3×6-in. card that contains a processor, a μ-Law codec, external RAM, and external ROM. Evaluation units for a TMS320C25 voice computer card cost $1500. Evaluation units for a voice module card containing a National 3200 family processor cost $500. EDN

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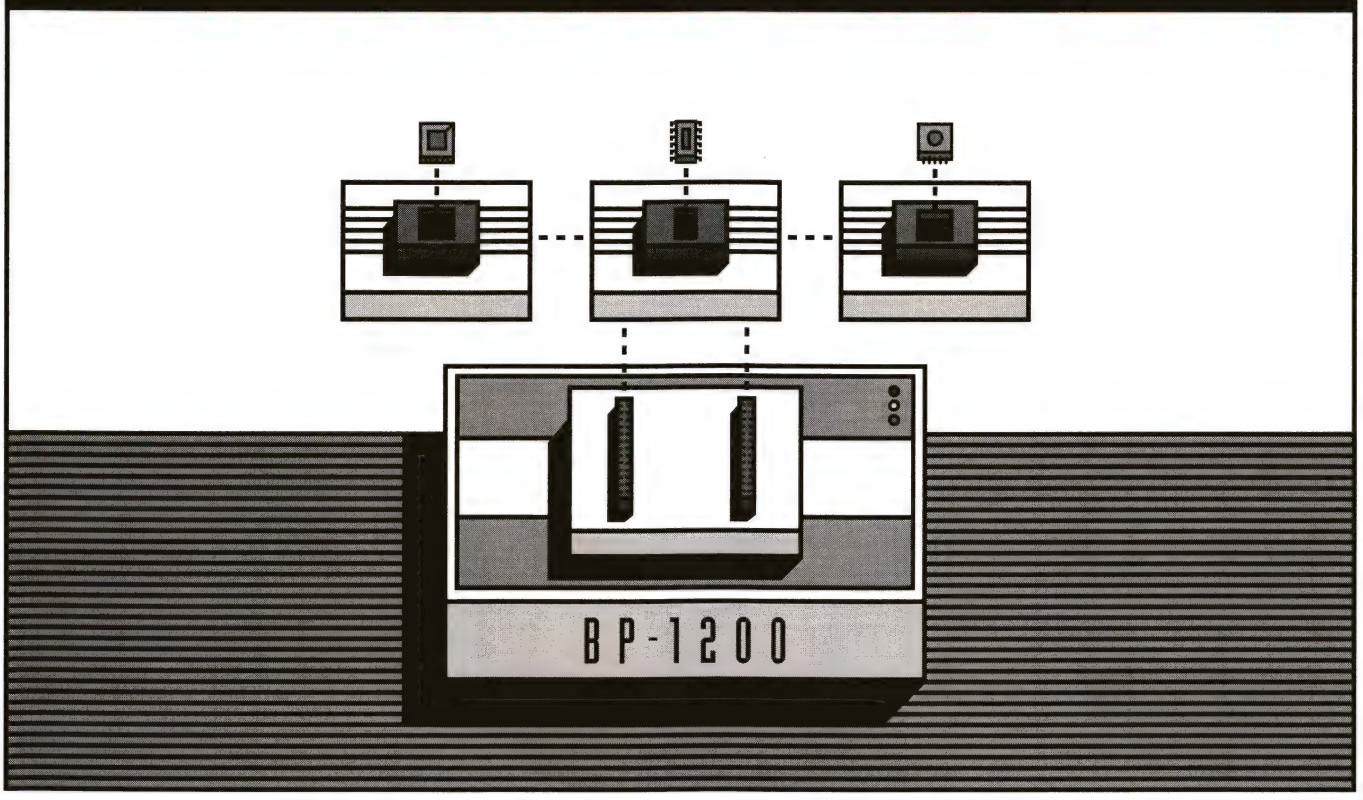

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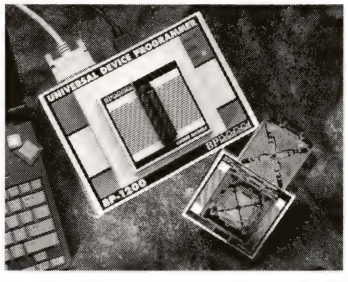

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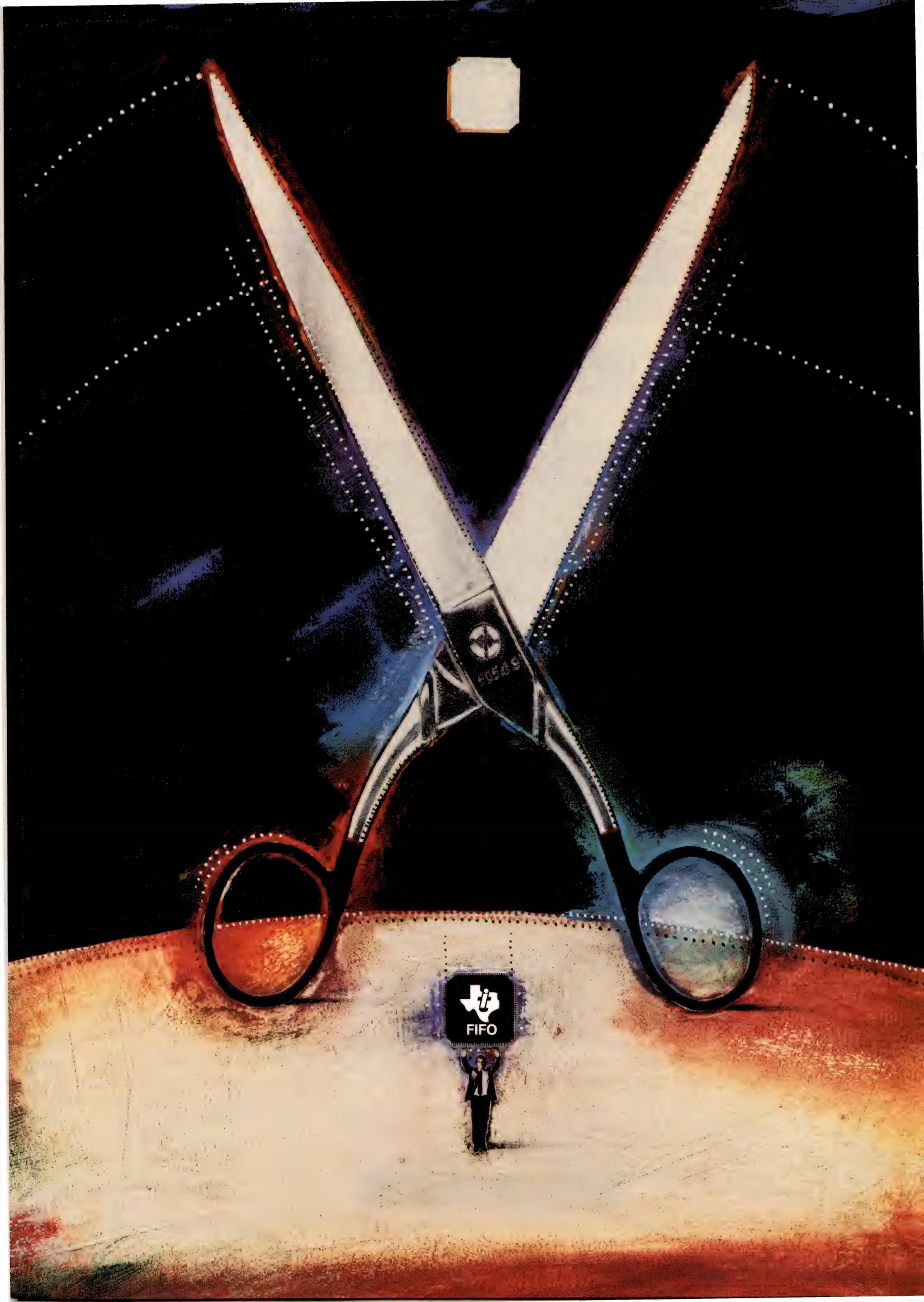
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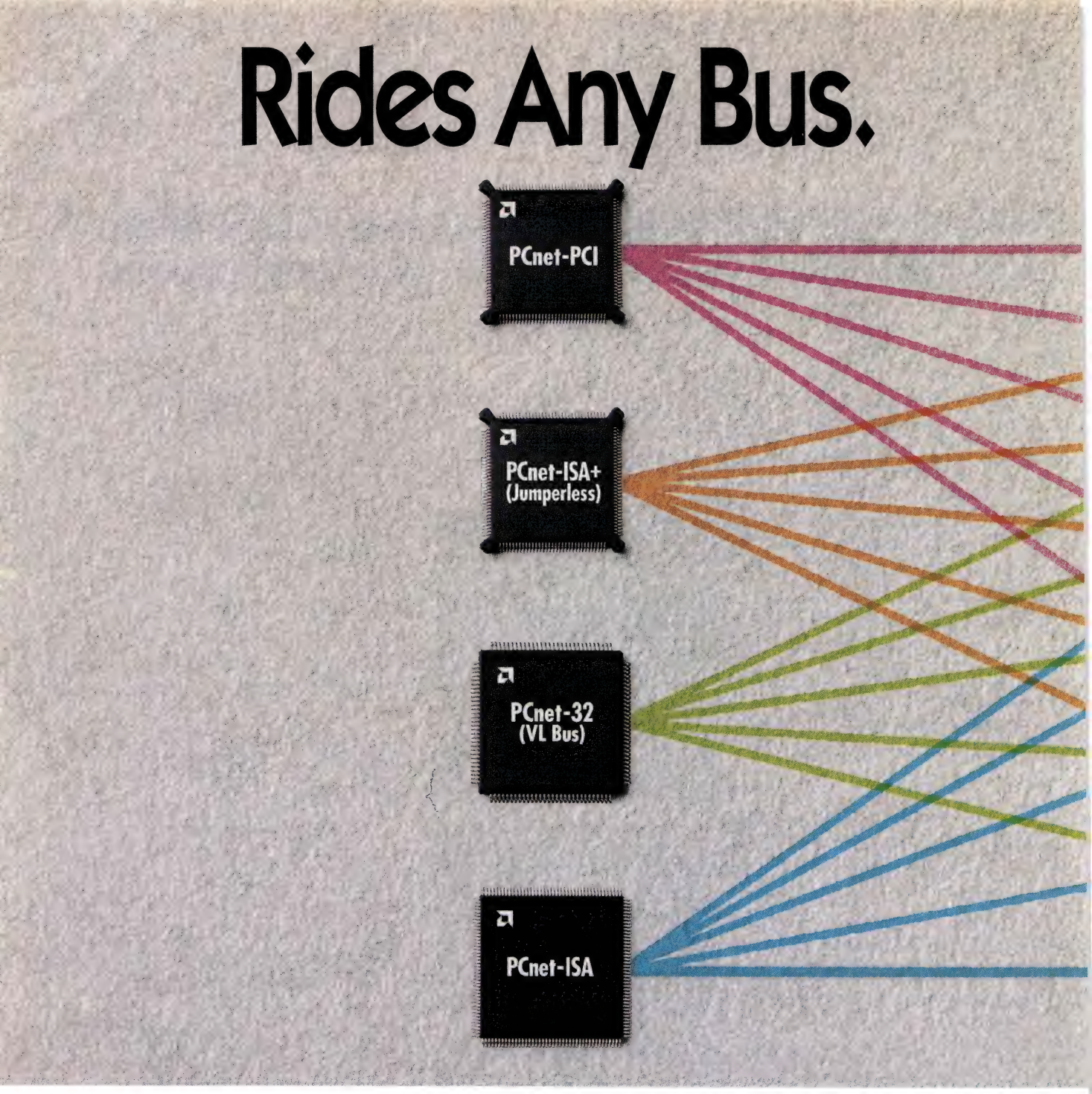

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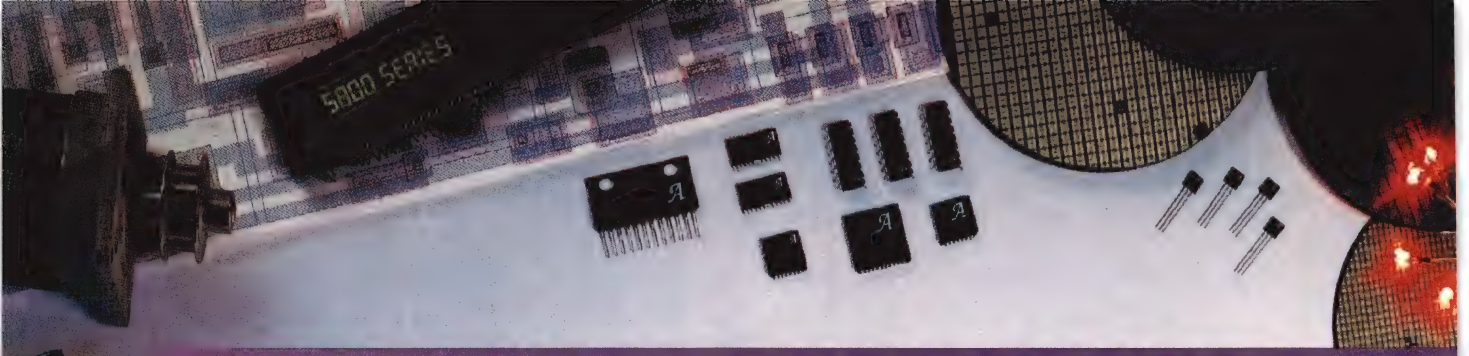

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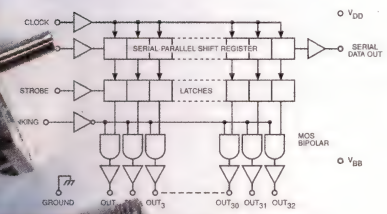

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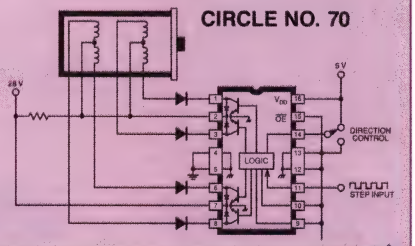

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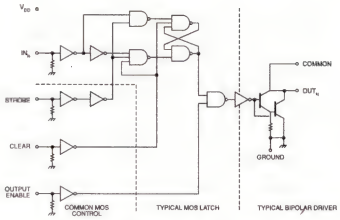

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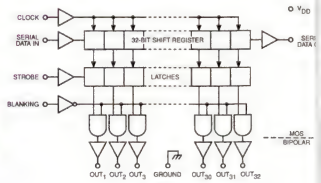

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Shrinking devices put the squeeze on system packaging

CHARLES H SMALL, Senior Technical Editor

While solving today's system-packaging puzzles, you can design products that are not only smaller but more reliable.

The trick to turning today's packaging problems into challenges is to shrink your product's parts count—not just its size—thereby increasing reliability **(Ref 1)**. Simply deleting parts from your system haphazardly (often called "Muntzing") can lower costs but also can scuttle your system's reliability.

Packaging problems arise simply because electronic devices are simultaneously getting smaller, faster, and more complex. Even inductor makers, such as Pico Electronics and Coiltronics, now offer surface-mount coils and transformers. These developments concentrate heat sources and ordain more connections in a smaller area.

As digital-clock speeds inexorably push beyond 50 MHz, transmission-line effects dominate the signal integrity of such systems. Higher clock speeds tax the signal integrity of pc boards, cables, and connectors.

Consumer demand plays a part, too. Users expect your new products to be more flexible and powerful than your old products were. Yet they also want your new products to fit into smaller, lighter packages and run twice as long as before on battery power.

New-age packaging

Motorola's new Series 900 VMEbus computers provide several examples of how to reduce costs while increasing reliability. The personnel Motorola employed in the computers' development also provides a lesson for management.

Motorola's computer-system designers ran into an all-too-common marketing problem: Motorola's customers could not forecast precisely which computers they would need. So the new system needed to be as flexible as possible. "No problem," you say. "Electronic engineers have always designed modular products." But Motorola decided that, along with being modular, the new computers would use as few parts as possible. After all, every part provides a chance for error.

The resulting design (**Fig 1**) required innovative electronic engineering. Where the old line had 600 parts, the new computers have only 190 parts. For example, this VMEbus system has no backplane; instead the cards simply stack using conventional connectors. Unfortunately, Motorola is not

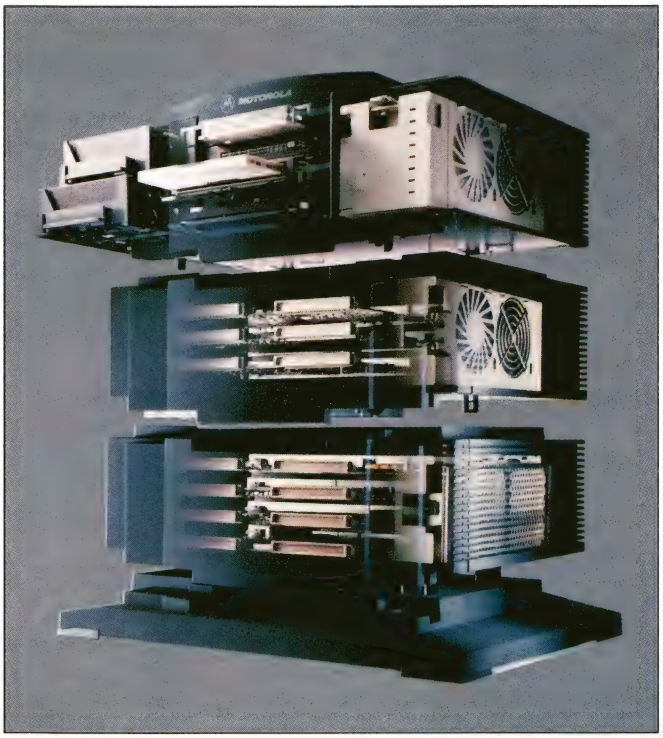

Fig 1—Innovative packaging has sharply reduced the number of mechanical components in Motorola's Series 900 VMEbus computers.

SYSTEM PACKAGING

disclosing how it made the stacking cards meet the VMEbus spec. (Connector manufacturers, such as Augat, happily provide you with Spice models for their connectors so that you can attempt to duplicate Motorola's feat.)

The computer also incorporates clever inputs from novel members of the design team: experts in molding plastic. If you remove the nonstructural plastic case of a conventional PC, you see several sturdy sheet-metal subframes cradling various parts of the computer. Lots of sheet-metal screws fasten this Erector-set assembly together. Wires and cables also abound, as do clamps and brackets to hold them.

In contrast, Motorola's plastics engineers made the plastic cases structural. They also provided molded-in supports wherever possible, dramatically reducing the mechanical parts count. Eschewing nuts, bolts, and screws, the designers made virtually every component snap into place—even the power supply. Simple, light-gauge sheet-metal cabinet liners serve only as RF shielding and also snap into place. Motorola's old line had 300 fasteners and 50 wires and cables. The new computers have only eight fasteners and two cables.

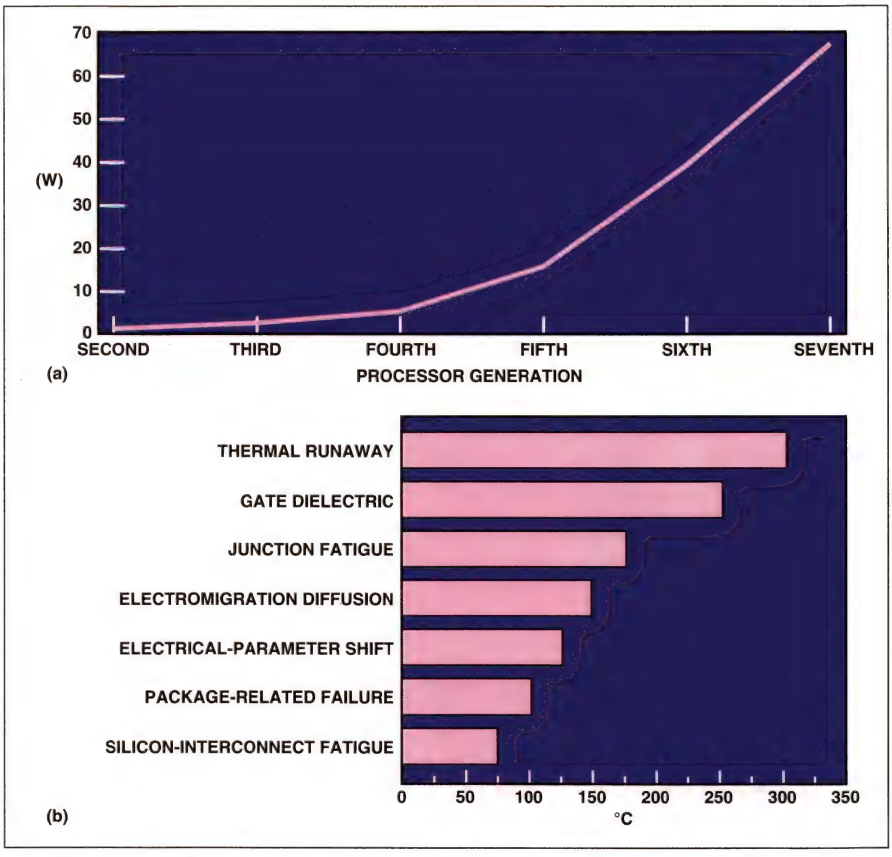

Fig 2—The graph in (a) shows that as clock speed climb, so does power dissipation. The graph in (b) shows the relationship between overtemperature and various kinds of failures. (Courtesy of Aavid Engineering)

Solving the world's toughest electronics packaging problem

A couple of specs tell you more than you would ever want to know about the terrifying packaging problems facing the Cray III's designers: A 4-processor Cray III has 62,738 GaAs ICs running at a clock speed of 480 MHz and dissipating 90 kW in a machine the size of a washing machine.

For starters, the designers did not fasten the custom GaAs ICs to the surface of the supercomputer's petite (25×25-mm) pc boards. Instead, each chip has gold bonding wires that stand vertically to the chip's surface. Then, machinery inserts the wires into holes on the pc board and swages the wires into place, leaving the chip standing on little stilts a tiny bit above the board's surface. This way, cooling can get to both sides of the chips.

After stacking boards into modules, ingenious "pins," rather than conventional connectors, make board-to-board contact vertically within the module (**Fig A**). The pins provide electrically fast and clean connections. Machinery tightly twists several strands of gold-plated beryllium-copper wire into a diminutive rope, or "pin."

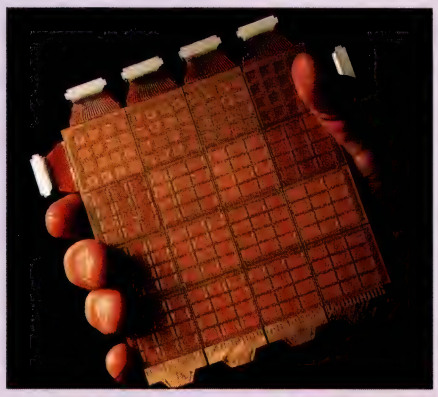

Fig A—The Cray III vertically stacks assemblies of 16 tiny, 1-in.-square pc boards into modules. Special "pins" connect the assemblies vertically. Comprising many such modules, the complete computer runs submerged in a cooling bath of Fluorinert.

At precise intervals, the machinery then untwists the wires, forming a springy, basket-like lump in the pin. Last, the machinery pulls these pins down through a stack of pc boards where the untwisted sections form a gas-tight seal with plated holes in the pc boards. Preserving signal integrity, flexible circuit boards make I/O connections from module to module. (Contact Rogers Corp for information on flexible circuit boards.)

Lastly, and heroically, designers dunked the entire supercomputer into Fluorinert to provide cooling. Pumps circulate the Fluorinert through the modules and around the ICs to pick up heat. The Fluorinert then goes to a remote chiller before being cycled back to the supercomputer.

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Reducing a chassis's parts count doesn't necessarily mean switching to plastic. Triple E Corp's Triple E card cage significantly reduces the number of parts in a card cage without abandoning all-metal construction. The company assembles VMEbus, VXIbus, Multibus II, Futurebus, AT, and EISA card cages from just five pieces: three extrusions and two stampings.

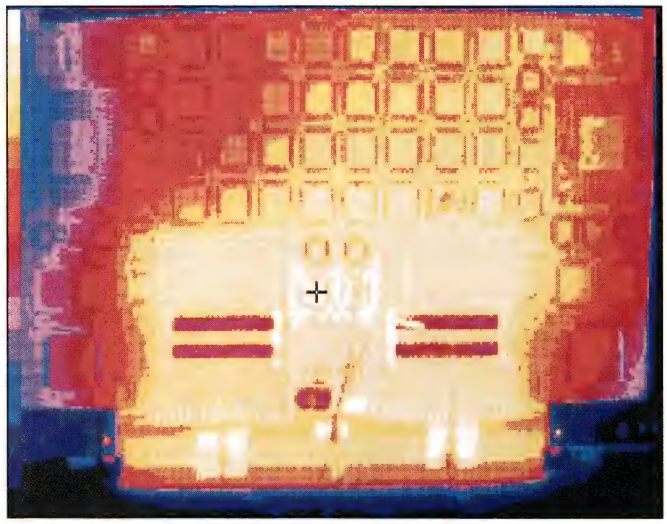


Fig 3—This pc board contains two heat-sinked Pentium μPs, which occupy the yellow areas having two red bars. The image renders the coolest parts of the board in blue, dropping down through the spectrum, through red and then yellow, to white for the hottest portions. Forced air flows across this board from left to right. (Courtesy of Compix)

Powerful or flexible?

Although some soothsayers and pundits envision all-in-one electronics products, such as a combination TV, phone, encyclopedia, and facsimile machine, users have shown themselves willing to customize products themselves. However, other than mucking out your own septic tank, it's hard to imagine a more user-hostile chore than installing a so-called "adapter" into a PC. Yet, PC users have bought an amazing number and variety of add-in pc boards.

You could make your product more flexible by designing with expensive in-circuit-programmable logic. Or you could try Free Frame Technologies' T-Modules, which comprise stacks of conventional circuit boards. Users can swap T-Modules in and out of small computers without fooling with screws or cables. Cutouts in the case locate one end of the modules, and the other end slips into a mother-board socket. Spring strips on the lid of the computer's case hold the modules in place.

Just like the designers of the T-Module, you can substitute board-to-board "mezzanine" connectors for cables. Connector manufacturers are competing to see who can make the lowest profile connector. Samtec Micro Stripe connectors consist of alternating layers of conductive and nonconductive silicon rubber. The connectors can match 0.020-in. pc-board pad spacing and connect two pc boards that are 0.125 in. apart. Specialty Electronics offers 1-mm receptacles, pin headers, and shunts that rise 0.067 in. above the pc board. Augat's Millipede surface-mount 1-mm connectors rise 0.116 in. (female) and 0.130 (male) above the pc board. Surface-mount connectors are much less noisy than through-hole connectors.

You can also mount components on board that were once chassis mounted, eliminating further wiring. Examples are Wickman's surface-mount and through-hole fuses, which eliminate the use of a fuse holder and its attendant wiring. Oxley's 2-part lamp comprises a panel-mounted lens that mates to a pc-board-mounted LED, again eliminating panel wiring.

Heat problems haunt small designs

"Thermal management"—a fancy term for keeping your product from burning up—is the bugaboo that constantly haunts shrinking designs. Never forget that every 10°C rise in operating temperature roughly doubles your product's failure rate.

Fig 2a illustrates the effects of increasing temperature. The new Pentium μP typifies today's high-speed, complex digital devices **(Fig 2b)**. Notebook-computer makers would love to ship Pentium-equipped products. Unfortunately for them, a 66-MHz Pentium dissipates more wattage than the notebook computers' thin packages can conduct to the outside world.

Fig 3 shows a pc-board containing two heat-sinked Pentium μPs. The image renders the coolest parts of the board in blue, dropping down through

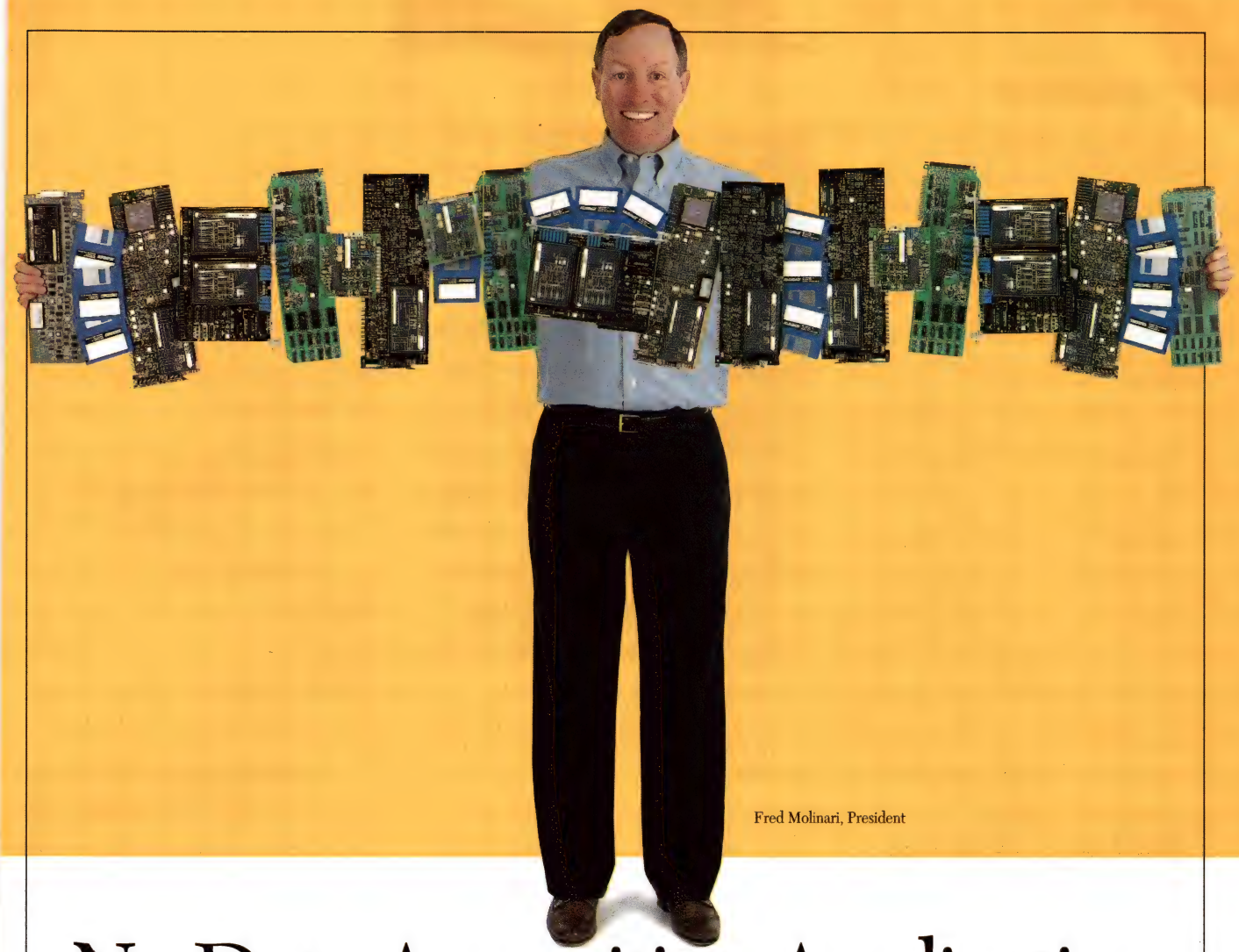
Looking ahead

First and foremost, the so-far inexorable increase in μP clock rates will continue to flog digital engineers, causing them to brush up on their transmission-line theory. And users will demand that PCs provide features such as multimedia and character recognition. Voice I/O and other forms of signal-processing will drive analog engineers into the digital domain. RF engineers will be busy designing the small, portable products that will set the 900-MHz band buzzing with wireless-network traffic.

Packaging will obviously have no choice other than to become denser. Today's peripheral connections to ICs will first give way to 2-D schemes along the lines of IBM's "flip-chip" technology. Ultimately, pc-board designers will have to enter the third dimension by stacking ICs. Or IC makers will have to produce 3-D (multiple-layer) devices.

These high clock speeds and 3-D designs present an interesting challenge to circuit-simulator makers, which have heretofore had to handle only low-speed, planar circuits.

To contend with finer lines and more layers, pc-board makers will have to adopt Star Wars technology. Vacuum deposition of thin-film traces and laser-drilled vias are techniques that could replace today's mechanical and chemical pc-board methods. The methods that a few multichip modules (MCMs) use today will become commonplace throughout the industry.



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the spectrum, through red and then yellow, to white for the hottest portions. Forced air flows across this board from left to right.

The two Pentiums occupy the large yellow area. Each Pentium has a pair of horizontal, equals-sign-like red bars (an artifact of their heat sinks). Between the Pentiums (and perhaps difficult to discern) is a white-hot component eclipsed by the Pentiums' tall heat sinks. In other words, the thermal management of this board needs more work.

Computers larger than notebook computers can use new products, such as Berquist's double-coated, heat-conducting tape to mount heat sinks on top of large devices, such as the Pentium μP. The electrically insulating tape readily conducts heat. Just as important, the tape eliminates the use of mounting hardware for the heat sink, reducing the pc-board's mechanical parts count. And, if a simple heat sink is not enough, IREC's tiny muffin fans can bring forced-air cooling right down to the device level.

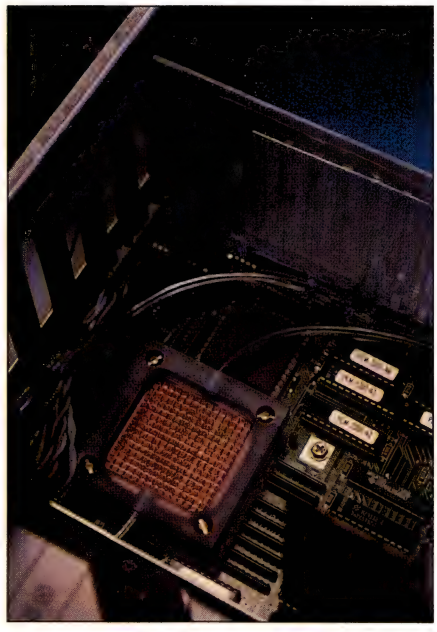

Fig 4—Future high-speed digital devices may require liquid cooling, such as this passive, thermosiphon system from Aavid provides.

Sweating the details

For really tight packaging, Aavid is developing liquid-cooled heat sinks. **Fig 4** shows such a thermosiphon heat sink attached to a Pentium. The liquid-tight heat sink transfers heat to the Fluorinert liquid. This liquid boils at very low temperatures, absorbing considerable heat as it changes phase. The Fluorinert vapor rises to an external radiator. After condensing in the radiator, the now-liquid Fluorinert flows back into the heat sink. The company is also working on much simpler and cheaper schemes involving sealing Fluorinert in a tough, electrically insulating plastic bag. Part of such a bag would simply rest on hot devices and conduct heat to cooler parts of a system.

IC makers are not the only ones shrinking components. Motorola has shrunk devices at the lowest level of active electronics. The MUN2111/2211 series of "bias-resistor" transistors integrate a bias-resistor network into the transistors' tiny SC-59 surface-mount package. Using these devices brings down the component count and the real estate consumed, but not the heat dissipated.

Ohmite has shrunk even the humble power resistor, providing a compact but concentrated source of heat that you must somehow remove. Ohmite screens some models of its power resistors onto a thermally conductive ceramic substrate. Other models use an even more thermally conductive, enameled, porcelain-coated steel substrate. The ceramic-substrate resistors can dissipate 10W/in.^{2}, and the steel-substrate resistors can dissipate 20W/in.^{2}. The planar construction results in low inductance (50 nH at 1 MHz typ).

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1. Nordwall, Bruce D, "Companies Reduce Solder to Increase Reliability," *Aviation Week & Space Technology*, December 6, 1993, pg 50.

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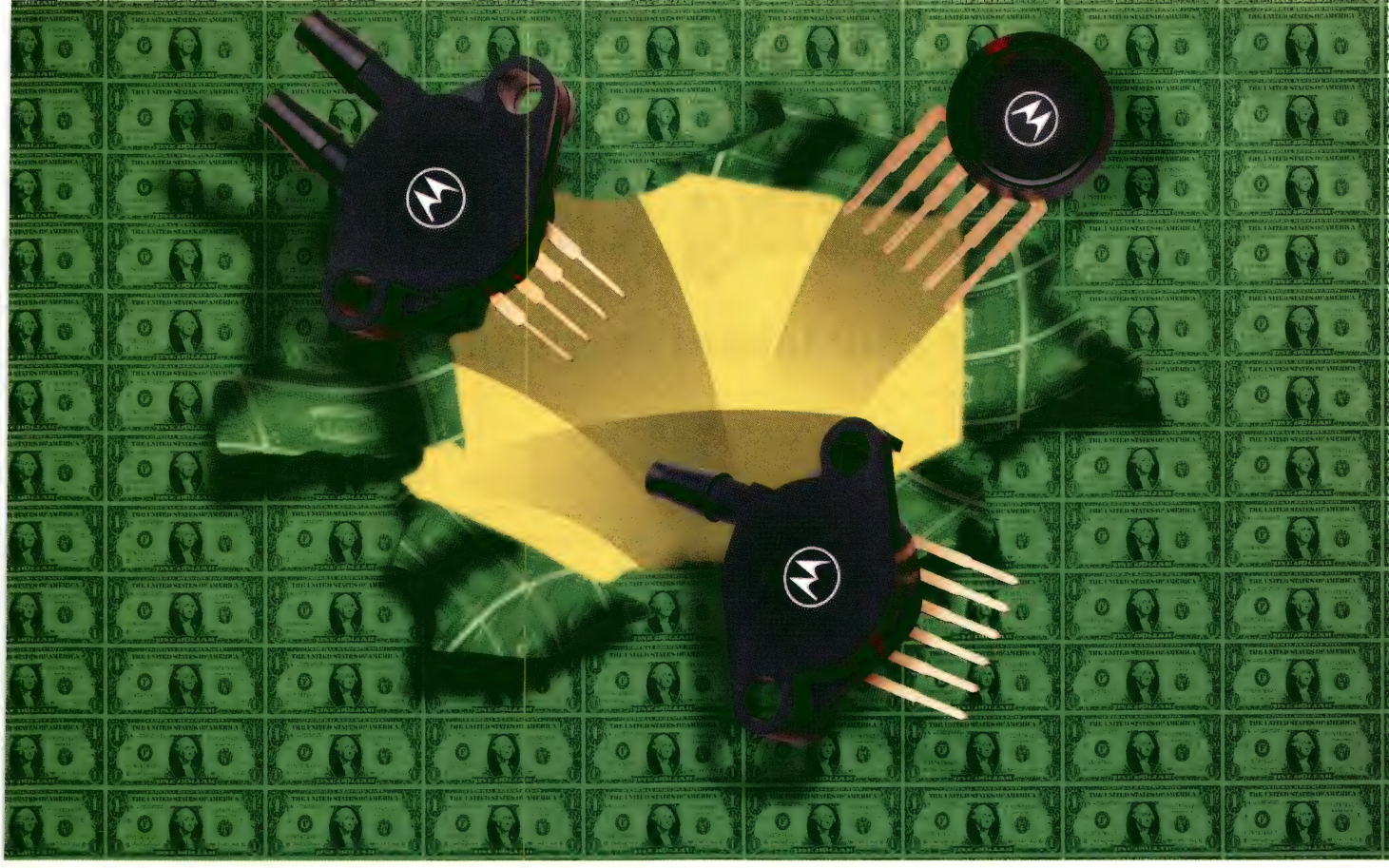

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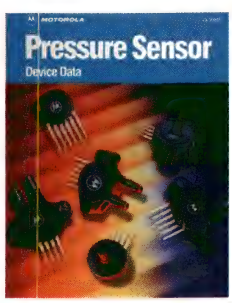

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Minimizing Clock Skew

Unique chip layout technique from OKI

OKI Semiconductor employs an integrated development environment in which the positions and sizes of clock drivers and trunk lines are determined by floor plan and flip-flop placement. This innovative approach has allowed the Sunnyvale, CA ASIC manufacturer to take the lead in minimizing RC loading variances. In fact, OKI guarantees a worst-case clock skew of 1.0 ns; 0.5 ns typical.

The OKI technique, which applies to all 0.8 μm ASIC products, lets you balance loading distribution among clock trunk lines at the layout stage plus gives you the flexibility to handle a wide array of design requirements. Such requirements can include multi-phase clocks, mega-macro blocks, a broad choice of floor plans, and more.

Current practice

Most chip designers still address the clock skew problem using one of two approaches: the multi-level tree method or the clock trunk technique.

The problem with multi-level trees is that the multi-level drivers create unwanted delays and frequently exhibit inconsistent driving capabilities.

In the clock-trunk approach, single-level clock drivers have wired outputs and run all the flip-flops through wide trunk lines. While this can solve the problems of the multi-tree approach, the clock drivers and trunk lines are embedded in the base array, restricting positioning and causing new balance-loading concerns.

OKI's answer: flexible clock trunks

The OKI solution is an automated layout technique that is entirely transparent to the designer. It centers around a flexible, single-level clock trunk approach in which the positions of the clock drivers and trunk lines are driven by the layout software. The advantages of this approach are twofold...

First, the software generates clock trunk lines on the basis of flip-flop distribution, *after* placement, making easy load-balancing possible among the trunk lines. Second, with the OKI solution, you can work with a large variety of design styles used in IC layouts.

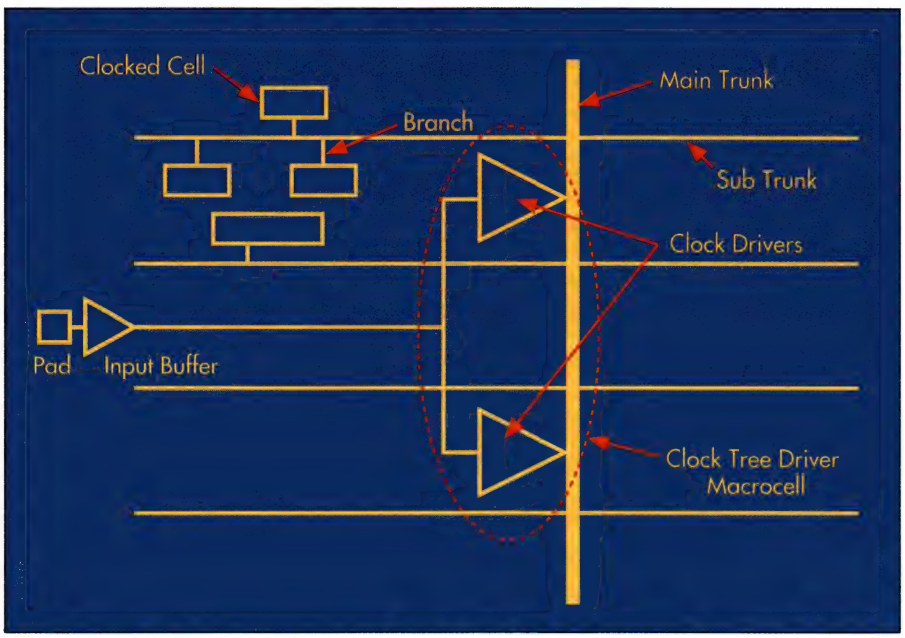


Figure 1. OKI's Clock Tree Structure

Clock driver structure

Figure 1 is a layout showing OKI's unique clock-handling structure. A vertical clock driver – composed of a number of output transistors and having a common output terminal from which trunk lines run horizontally – is placed inside the core area. (The *logical* macrocell, as opposed to the physical structure, is a simple, *one-component* logic model in your netlist.) Each flip-flop connects to a clock trunk via short, minimum-width branch wires.

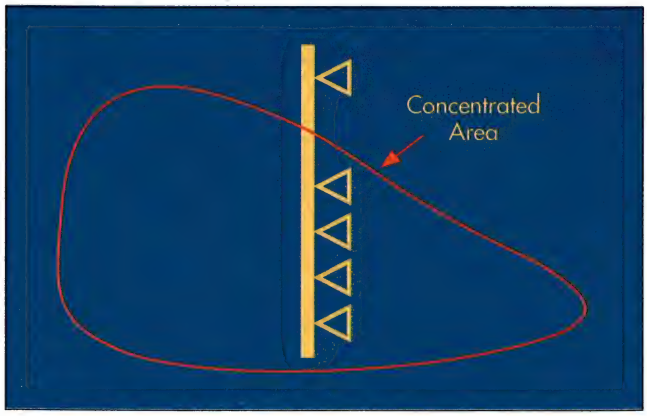


Figure 2. Dynamic Clock Driver Placement

Floor plan placement & clock trunk generation

After a floor planning session using OKI's floor planning tool, you initiate a layout session in which all the components in the design area are automatically placed without regard for clock nets.

The positions and sizes of clock drivers and the sizes of the clock trunk lines are determined by the particulars of the floor plan. The OKI layout software automatically generates an appropriate number of clock trunk lines based upon flip-flop distribution. A higher concentration of trunk lines is dynamically generated (where the lines are needed most) so that loading capacitance and resistance are equally distributed. [See Figures 2 and 3.]

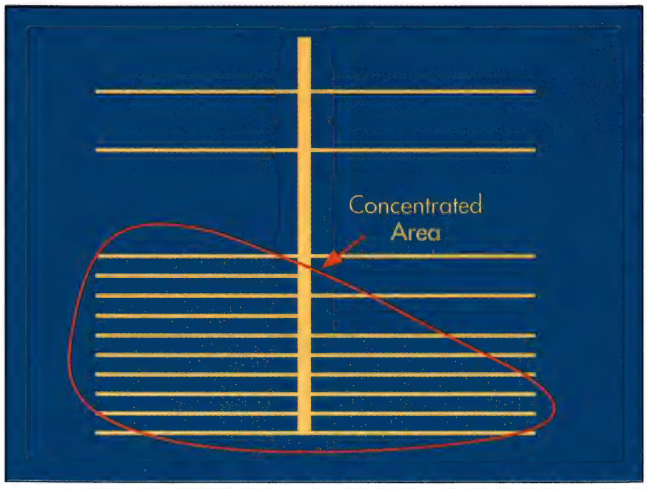


Figure 3. Dynamic Sub-trunk Allocation

Flip-flops are allocated to the trunk lines so that no single line has a greater load. At this point, flip-flop placement is further optimized to reduce layout interconnect. Finally, minimum-length branch nets are routed to each flip-flop, further reducing and balancing clock loading.

Performance benefits

Several factors influence clock performance (speed and skew). These include the driving capability of the clock driver; the fan-out loading capacitance connectable to each clock line; and the parasitic capacitance and resistance existing in the layout interconnect between the clock driver and the individual flip-flops.

The cumulative effect of these implementations is to minimize all resistance and capacitance variances. In this way, OKI is able to guarantee minimum clock skew.

To achieve highest performance, OKI has analyzed the range of capacitance and resistance on given die sizes, defining limits for our clock drivers so that the maximum capacitance and resistance on any one clock trunk are not exceeded. These limits, expressed in terms of maximum fan-out loading, are automatically implemented in the new OKI layout technique.

To further assure top performance, routing restrictions, minimizing the length of branch wires, are defined. The cumulative effect of these implementations is to minimize all resistance and capacitance variances. In this way, OKI is able to guarantee minimum clock skew.

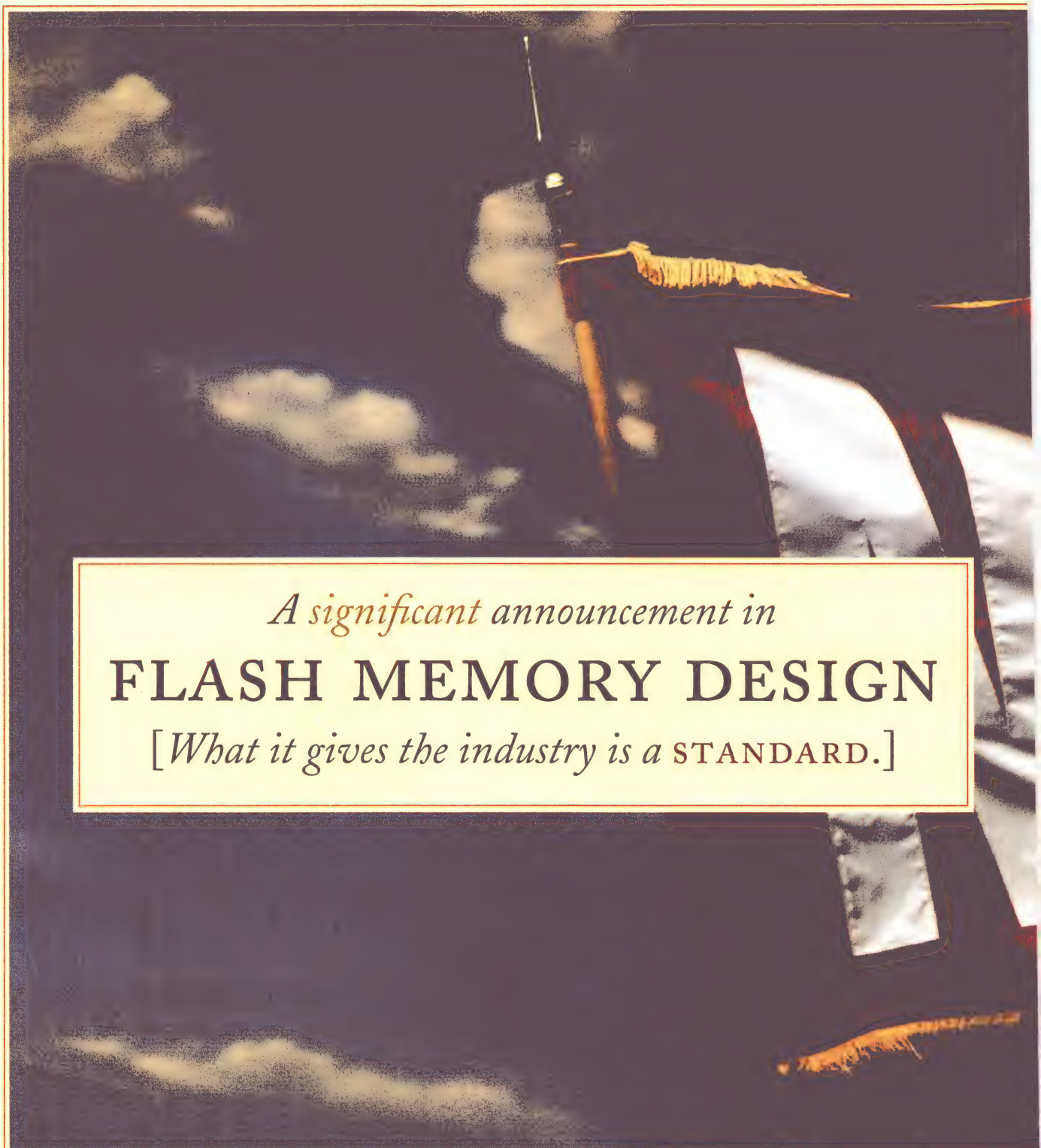
Exceptional test results

OKI has conducted numerous studies on 0.8 µm designs using the new layout technique. In each case, the RC circuits of the clock nets were extracted and clock skew checked and verified by an HSPICE* circuit simulator. The results were excellent. In all the tests, the greatest skew obtained was 0.47 ns – a showing that further confirms the value of the OKI technique in which the positions of clock drivers and clock trunk lines are flexibly generated. ■

*A trademark of Meta-Software, Inc.

For an application note and a copy of the complete technical paper treating the OKI method of reducing clock skew, call (800) OKI-6388, and ask for Literature Package # 017. For more information from an OKI engineer, call Steve Lapham, (408) 737-6337.

For more information circle 12



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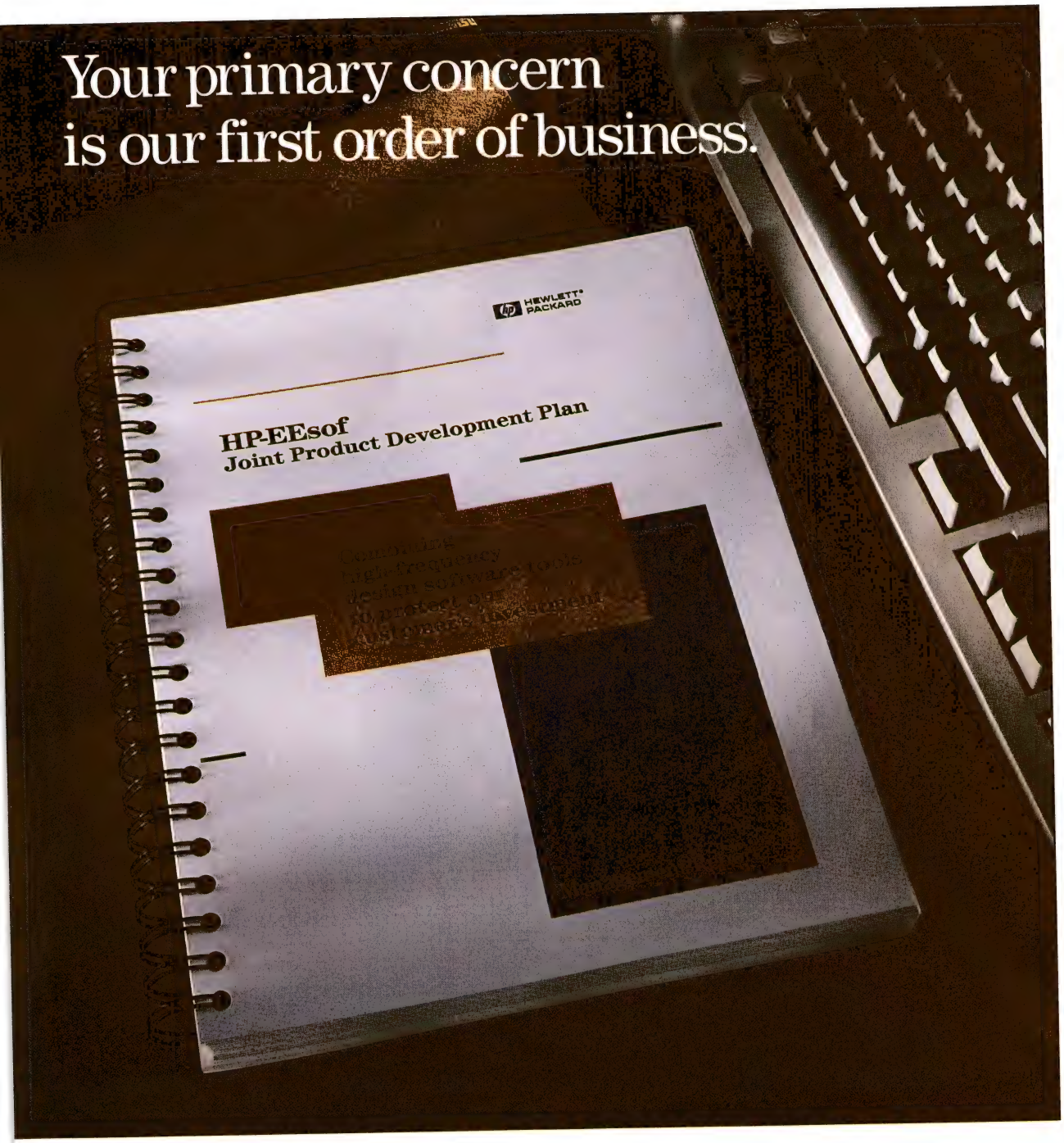

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LINEAR TECHNOLOGY

DESIGN NOTES

Single 4-Input IC Gives Over 90dB Crosstalk Rejection at10MHz and is Expandable – Design Note 79

John Wright

Introduction

Professional video systems need to multiplex between many signals without interference from adjacent video sources that are not selected. Final system crosstalk rejection of all non-selected or "Hostile" signals of 72dB is regarded as "professional quality." This level of isolation is very difficult to achieve because every doubling in the number of inputs degrades the crosstalk by 6dB. In the past because no single IC was good enough, cascades of discrete switches and amplifiers were used to achieve the necessary isolation. An additional requirement of some video multiplexers is the ability to switch quickly and cleanly so the sources can be changed in picture without visible lines or distortion. New emerging multimedia systems require the performance of professional systems in the PC environment.

The new LT1204 four-input video multiplexer IC speeds the design of high performance video selection products. It features easy input expansion, and over 90dB crosstalk rejection on a PC board up to 10MHz even when expanded to 16 inputs. Additionally, this new multiplexer has low switching transients and includes a 75MHz current feedback amplifier to drive 75Ω cables. Figure 1 shows the LT1204 in a typical application.

Expanding the Number of Inputs

To expand the number of MUX inputs LT1204s can be paralleled by shorting their outputs together. The Disable feature ensures that amplifier outputs that are not selected do not alter the cable termination. When the LT1204 is disabled (pin 11 low), the output stage is turned off and the feedback resistors are bootstrapped, effectively removing them from the circuit. This has the effect of raising the "true" output impedance to about 25k in Figure 1. The LT1204 disable logic has been designed to prevent shoot-through current when two or more amplifiers have their outputs shorted together. The LT1204 also has a logic controlled shutdown (pin 12 low) that drops the supply current from 19mA to 1.5mA. When shut down, the feedback resistors load the output because the bootstrapping is inoperative. Figure 2 shows this loading effect for a 16-to-1 MUX made with four LT1204s using the Disable feature vs the Shutdown feature.

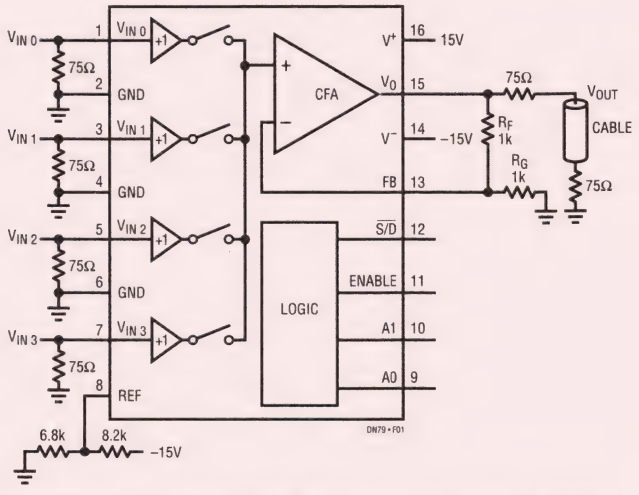


Figure 1. 4-Input Video Multiplexer with Cable Driver

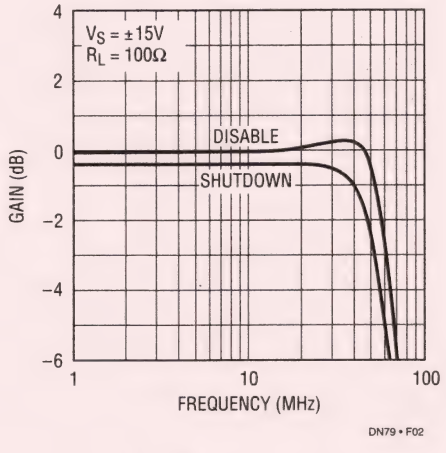
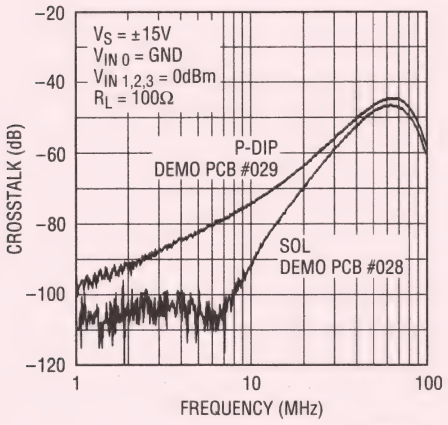


Figure 2. 16-to-1 Multiplexer Response Using Disable Feature vs Shutdown Feature

PC Board Layouts

Crosstalk is a strong function of the IC package, the PC board layout, as well as the IC design. Layout of a PC board that has over 90dB crosstalk rejection at 10MHz is not trivial. PC boards have been fabricated to show the component and ground placement required to attain this level of performance. It has been found empirically from these PC boards that capacitive coupling across the package of greater than 3fF (0.003pF) will diminish the rejection. Keys to the layout are: placing ground plane between inputs, minimizing the feedback pin trace length, putting feedback resistors on the back side of the surface mount PC board, and guarding pin 13 with ground plane.

Crosstalk in P-DIP and SOL vs Frequency

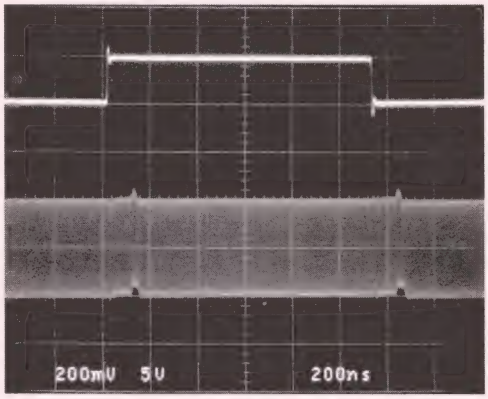


LT1204 • AI01

Switching Transients

Multimedia systems switch active video "in-picture" to create special effects and this requires fast clean transitions with low "glitch" energy. In the past video source selection was made during the blanking period and switching transients were not visible. The LT1204 has input buffers that isolate the internal make-before-break switches. These buffers ensure glitches are minimized at the inputs. This is important because loop-through connections send these glitches to other equipment. When two channels are on momentarily the more positive voltage passes through; if both are equal, there is only a 40mV error at the input of the CFA. The time of this 40mV error can be reduced by adjusting the voltage on the Reference (pin 8). The Reference pin is used to trade off positive input voltage range for switching time. On ±15V supplies, settling the voltage on pin 8 to −6.8V reduces the switching transient to a 50ns duration, and the positive input range reduces from 6V to 2.35V. The negative input range remains unchanged at −6V. Included are photos of the switching transients for the new LT1204 as well as competitive CMOS and bipolar MUXs.

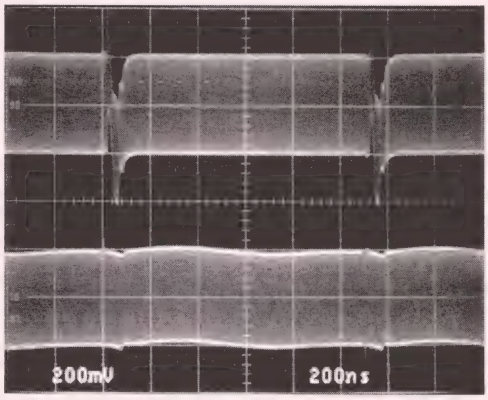
LT1204 Output Switching Transients



$V_{IN\ 0}$ AND $V_{IN\ 1}$ CONNECTED TO A 2MHz SINEWAVE
V_{REF} = −6.8V

DN79 • AI02

Competitive MUXs



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Priority encoders slip into FPGAs

Swapnajit Mittra, Baharat Electronics, Bangalore, India

The standard 8-to-3 priority encoder's design, in maximal canonical form (such as the 74148), suffers from drawbacks when you try to use the design as a macro in a large digital project. The drawbacks are

- The number of inputs to the gates varies from two to nine
- If any of the inputs develops a stuck-at-zero or stuck-at-one fault, such a fault is difficult to detect
- Reconfiguring the design to suit a fault-tolerant design is difficult.

The simplified approach in **Fig 1(a)** shows a 2-to-1 priority encoder, which generates the proper output as well as a signal-present output (SP). SP indicates the presence of any signal at the inputs, simplifying testing. By inspection, you can see that the circuit in **Fig 1(a)** is a priority encoder.

The circuit in **Fig 1b** combines two of **Fig 1(a)**'s basic building blocks into a 4-to-2 priority encoder. And, by extension, **Fig 2** shows an 8-to-3 encoder. Simulations show that this circuit has 98% fewer transistors than the canonical circuit does for cell-based design. Owing to never exceeding the number of inputs to a logic cell, this design also compiles economically over a Plessey gate array.

Extending this design to 16 or more inputs is not advisable. If you extend the design to 16 or more inputs, its critical path increases linearly with the number of inputs; the canonical approach always yields a 3-stage design, giving it superior propagation delay. **EDN BBS /DI_SIG #1370** EDN

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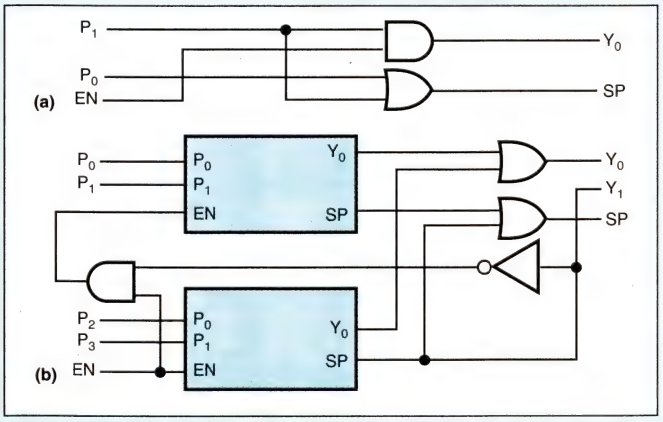

Fig 1—The simple 2-to-1 input priority encoder in (a) extends easily to a 4-to-2 priority encoder.

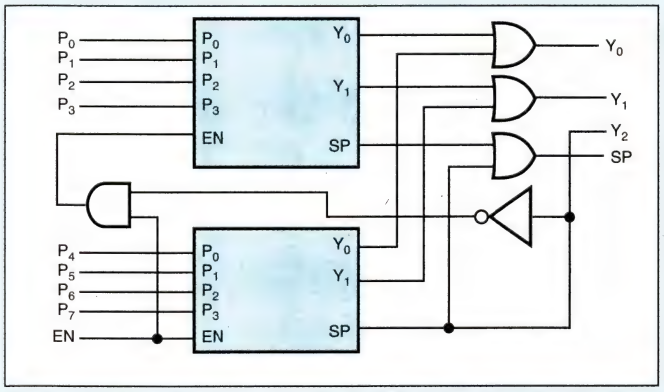

Fig 2—The 4-to-2 priority encoder in 1(b) is the basis for this 8-to-3 priority encoder. This design compiles over gate arrays and FPGAs more economically that does the cannonical design.

Off-line power supply requires few parts

Sam Ochi, IXYS Corp, Santa Clara, CA

The simple off-line power supply in **Fig 1** can provide 150 mA or less and uses only a handful of components. Current regulator, IC_1, acts as a preregulator for any of the popular 3-terminal regulators (The **figure** shows a 78L05). Because IC_1 drops most of the voltage in this circuit, the circuit suits only low-current applications.

To get the best possible power factor and simultaneously reduce IC_1's power dissipation, choose capacitor C_1, such that the lowest point of its ripple voltage is greater than voltage dropped across IC_1 and IC_2—even at your application's maximum load. **EDN BBS /DI_SIG #1364** EDN

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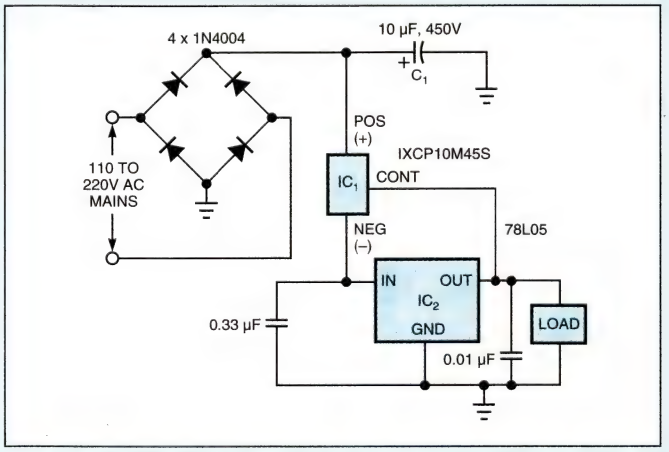

Fig 1—A current regulator feeds just the right amount of current to a common 3-terminal regulator, enabling this simple low-current power supply to operate directly from the mains.

VisualBasic does I/O

Jon Titus, *Test & Measurement World*, Newton, MA

Microsoft's VisualBasic—which runs under Windows—cannot operate on a PC's I/O ports. However, you can add dynamic-link libraries (DLLs) to extend the keywords of native VisualBasic (**Listing 1**). The compiled code, listings, and documentation in ZIPfile DI1167Z.ZIP (attached to EDN BBS /DI_SIG #1367) let you perform I/O operations using the new keywords *Inp* and *Out*. These added keywords operate the same way these keywords do in other Basic dialects.

To use *Inp* and *Out* in VisualBasic, you must tell your program that these operations exist. Use the *Declare* statements, as **Listing 2** shows. Remember that the *Out* operation is a subroutine because it simply outputs a byte; it returns nothing back to your VisualBasic program. The *Inp* operation is a function, because it returns a byte from an input port. You use the *ByVal* keyword to tell VisualBasic that you want it to transfer the actual value, and not a reference or pointer to the value.

In addition, you must explicitly tell VisualBasic where to find the library functions in your DLL. This example assumes the DLL is on a floppy disk in the B drive. You can put the DLL on another drive, but be sure to tell VisualBasic where it is.

Simple VisualBasic program fragments show how to use the *Inp* and *Out* instructions. For example, Out 771, 130 sends the value 130 to output port 771 of my PC. On the other hand, A=Inp(769) assigns the byte at input port 769 to variable A. The syntax is exactly the same as in most other Basics.

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Listing 1—C++ source code for DLL (Borland C++ compiler)

```
#include <d:\borlandc\include\windows.h>
#include <d:\borlandc\include\dos.h>

extern "C" {
int FAR PASCAL _export Test (int) ;
void FAR PASCAL _export Out (int, int) ;
int FAR PASCAL _export Inp (int) ;
}

int FAR PASCAL LibMain (HANDLE hInstance, WORD wDataSeg,
                WORD wHeapSize, LPSTR lpCmdLine)

     {
     hInstance = hInstance;
     wDataSeg = wDataSeg;
     wHeapSize = wHeapSize;
     lpCmdLine = lpCmdLine;

     if(wHeapSize > 0)
          UnlockData (0);
     return 1 ;
     }

int FAR PASCAL _export Test (int arg1)
{
     return (arg1 + 1);
}

void FAR PASCAL _export Out (int portaddr, int portdata)
{
     unsigned char data;
          outportb(portaddr,portdata);
}

int FAR PASCAL _export Inp (int portaddr)
{
     int portdata;
     portdata = inportb(portaddr);
     return (portdata);
}
```

Listing 2—VisualBasic location declarations

```
Declare Function Test Lib "b:\cuser2.dll" (ByVal Numb%) As Integer
Declare Sub Out Lib "b:\cuser2.dll" (ByVal Addr%, ByVal Byte%)
Declare Function Inp Lib "b:\cuser2.dll" (ByVal Addr%) As Integer
```

Motor-drive algorithm saves space and cycles

José A P Machado da Silva, University of Porto, Porto, Portugal

The algorithm embodied in the second subroutine in **Listing 1** generates the excitation sequence for most permanent-magnet and hybrid stepper motors. This subroutine is smaller than subroutines that spring from other algorithms.

To understand the algorithm, first consider that stepper motors have two stator coils, A and B, each having a center tap. Phase notation (A,A,B, and B) shows the direction of the current flow. That is, $AA=10_2$ symbolizes that current flows through half-coil A and that half-coil A is off.

To get the maximum torque from a stepper motor, you must drive two phases at a time. Using the binary notation developed in the preceding paragraph, the 4-phase drive sequence for all four half coils is 0101_2, 0110_2, 1010_2, 1001_2 or 5_{HEX}, 6_{HEX}, A_{HEX}, 9_{HEX}.

Listing 1—Stepper-motor drive subroutines

```
Memory Accessing
                                        bytes/cycles
Begin   MOV  Rr,curraddress               2/2        Load adr reg w/current
                                                       table address
New     MOV  Outpur,@ Rr                  2/2        Send drive sig to output
        INC  Rr                           1/1        Increment adr reg
        CJNE Rr,#lastaddress+1,More       3/2        Rel-cond jump to More
More    ...                               ...        Delay
        JNZ  New                          2/2        End of motion?
End     MOV  curraddress,Rr               2/2        Save adr reg

Accumulator Rotating

Begin   MOV  A,currstate                  2/1        Load A w/current drive
                                                       bytes
Next    MOV  Output,A                     2/1        Send drive sig to output
        RL   A                            1/1        Rotate A left twice
        RL   A                            1/1
        ...                               ...        Delay
        JNZ  Next                         2/2        End of motion?
End     MOV  curstate,A                   2/1        Save drive bytes
```

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Differential Nonlinearity	–0.95	±0.5	+0.95	–0.95	±0.5	+1.0	–0.95	±0.5	+1.25	LSB's
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* f_{in} = 2.45MHz

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The usual technique for generating this sequence with a μP is to look up the succeeding phase commands in a table (see the first subroutine in **Listing 1**). This operation requires a multibyte MOV instruction. The new algorithm obtains each phase by rotating the accumulator's contents (**Fig 1**). Thus, the algorithm saves processor cycles and the space needed for the table.

In **Fig 1**, the accumulator begins with $A5_{HEX}$. The accumulator's least-significant four bits are the motor-drive output (5_{HEX}). Two circular-rotate left instructions yield the next motor-drive output, 6_{HEX}, and so on. To drive the motor in the opposite direction, reverse the sense of the rotation instructions.

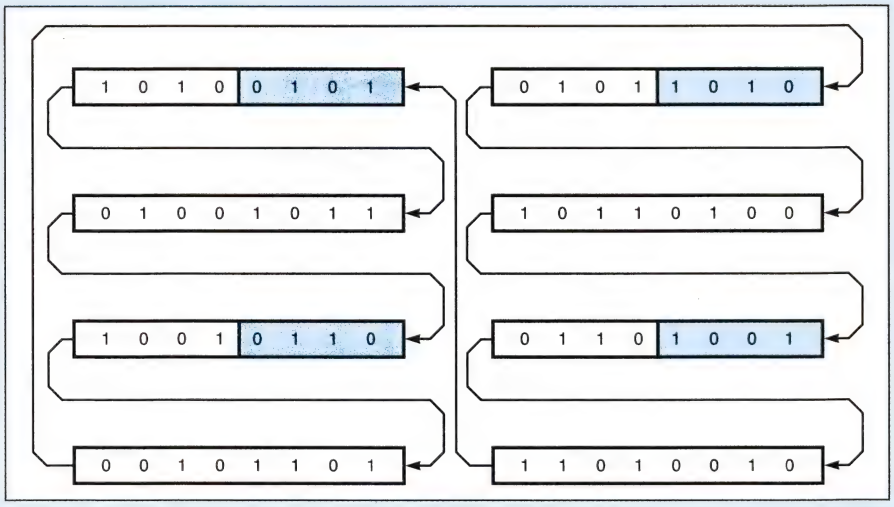

Fig 1—Rotating the proper bytes around the accumulator generates drive signals for a stepper motor.

Comparing the two subroutines in the **listing**, you can see that the accumulator-rotating algorithm saves 10 memory locations (six in the subroutine plus four in the table) and three μP cycles for each step.

You can use the same algorithm to generate wave-drive and half-step sequences. Rotate one of the bytes—48_{HEX}, 84_{HEX}, 23_{HEX}, or 12_{HEX}—to obtain wave drive. Obtain the sequence 0101_2, 0100_2, 0110_2, 0010_2, 1010_2, 1000_2, 1001_2, 0001_2 by alternately rotating both of the full-step sequences to achieve half-step drive, saving even more memory. EDN

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To Vote For This Design, Circle No. 344

Spice models CMOS switch

Paul E Brown Jr, McDonnell Douglas, Santa Ana, CA

BBS

The Spice subcircuit in **Listing 1** is a model of an spst CMOS analog switch. Ideal circuit elements such as PMOS and NMOS FETs model the switch (M3 and M4) and the switch's CMOS inverters (M1 and M2). Resistors and capacitors model the CMOS switch's drain-to-source on-resistance (RDS), its source capacitance (CS), and its drain capacitance (DC). An ideal dc-voltage source (VREF) and a voltage-controlled voltage source (E1) model the switch's logic-level voltage shifter.

The model employs parameter passing so that you can use the model for more than one type of switch. You can find the needed parameters on the switch manufacturer's data sheet. If you do not pass your own parameters, the model uses the defaults in the **listing**.

A typical call to this model is

XREF N1 N2 N3 N4 N5 N6 SWITCH {IS=xx ID=xx CS=xx CD=xx RDS=xx},

where N1 is the source node, N2 is the drain node, N3 is the control-voltage node, N4 is the positive power-supply voltage node, N5 is the power-supply return node, and N6 is the negative power-supply voltage node. You can find a copy of this **listing** on the EDN Readers' Bulletin Board as DI1366.LST.

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Listing 1—CMOS analog-switch Spice model

```
* IDEAL CMOS ANALOG SWITCH
* S = SOURCE; D = DRAIN; VL = LOGIC CONTROL VOLTAGE
* SWITCH IS OPEN FOR VL = 0V; SWITCH IS CLOSED FOR VL = 5V
*
* PASS THE FOLLOWING PARAMETERS
*
* IS  =  SOURCE LEAKAGE CURRENT IN AMPERES
* ID  =  DRAIN LEAKAGE CURRENT IN AMPERES
* CS  =  SOURCE OFF CAPACITANCE IN FARADS
* CD  =  DRAIN OFF CAPACITANCE IN FARADS
* RDS =  DRAIN TO SOURCE ON RESISTANCE IN OHMS
*
.SUBCKT SWITCH 2 3 1    4    5    6  {IS=1PA ID=1PA CS=1PF RDS=0.1}
*              S D VL  VCC  GND  VEE
R1    1 5 1T
R2    7 5 1T
T3    8 5 1T
VREF  7 5 -2.5V
E1    8 5 POLY(2) 1 5 7 5 0 6 6
R4    9 5 1T
C1    9 5 {CS}
RS    2 5 {1/IS}
CS    2 5 {CS}
RD    3 5 {1/ID}
CD    3 5 {CD}
RDS  10 3 {RDS}
M1    9 8 6 6 NMOS
M2    9 8 4 4 PMOS OFF
M3   10 9 2 4 PMOS OFF
M4   10 8 2 6 NMOS OFF
.MODEL PMOS PMOS(KP=10M)
.MODEL NMOS NMOS(KP=10M)
.ENDS
```

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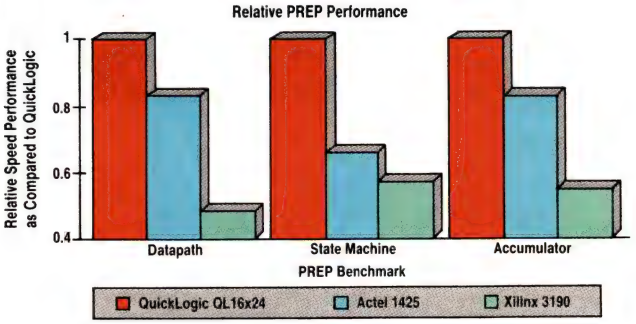

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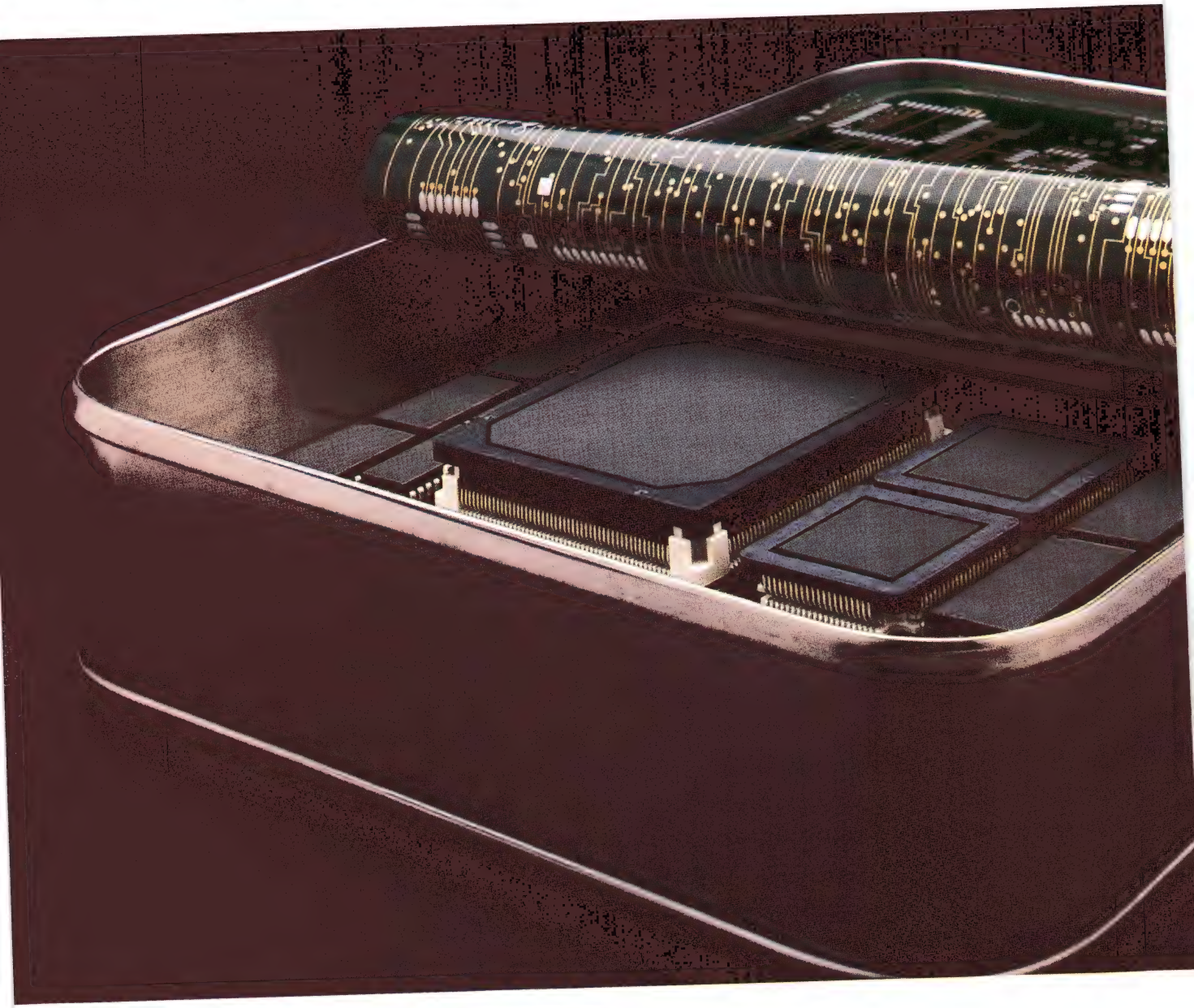

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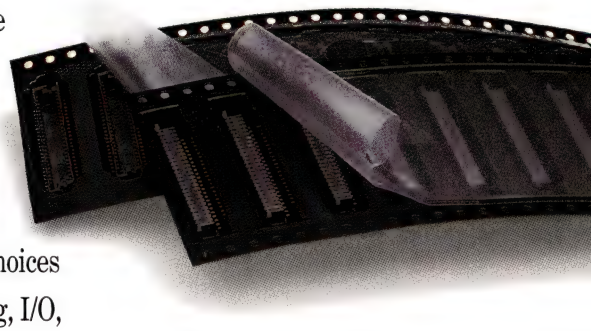

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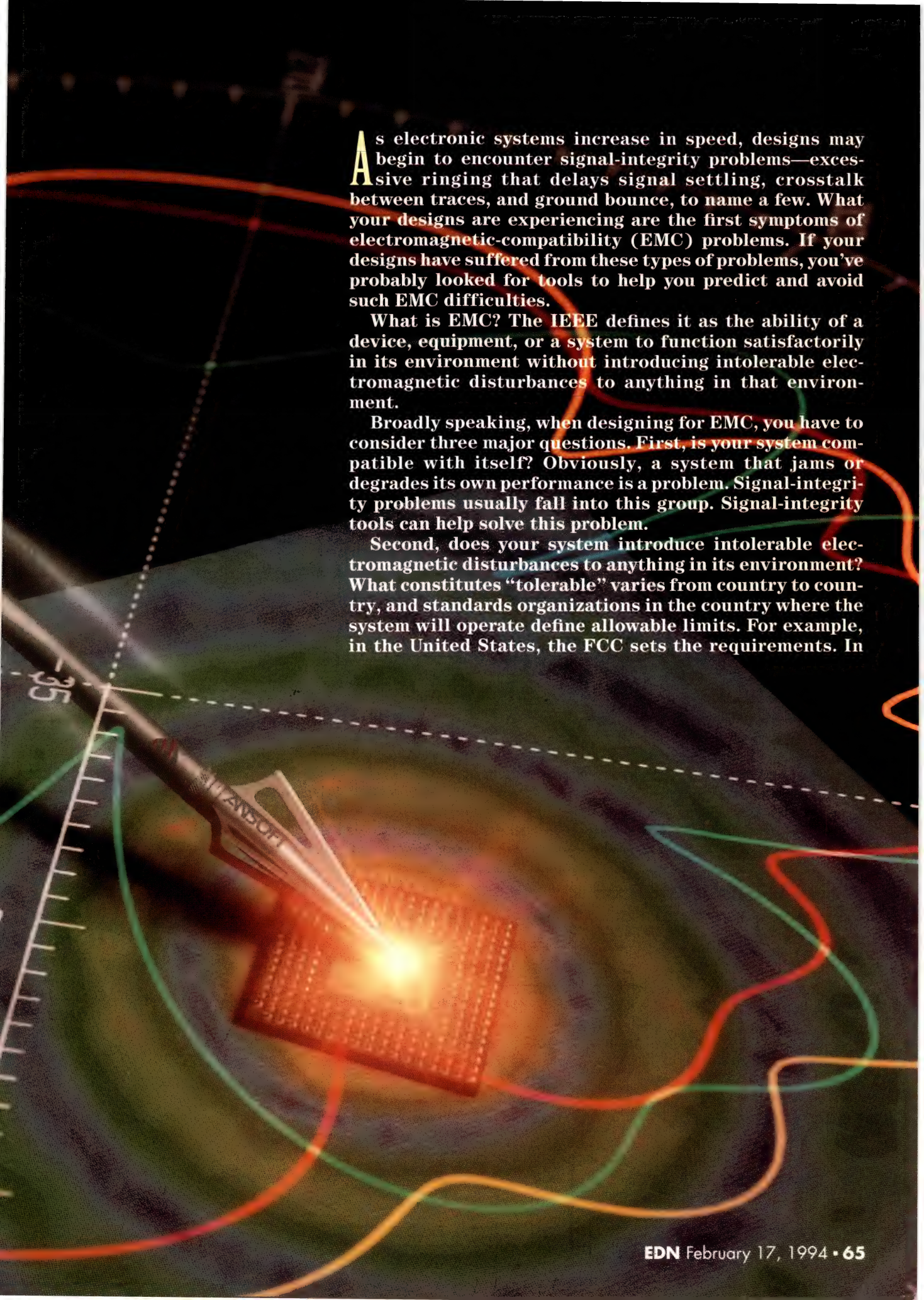
EMC-design tools

Doug Conner, Technical Editor

The problem facing designers of high-speed circuits is not just to make sure that products work by themselves. Designers must also make sure that their products fit into a larger community of electronic systems. The issue is electromagnetic compatibility (EMC).

Photo courtesy Ansoft Corporation



As electronic systems increase in speed, designs may begin to encounter signal-integrity problems—excessive ringing that delays signal settling, crosstalk between traces, and ground bounce, to name a few. What your designs are experiencing are the first symptoms of electromagnetic-compatibility (EMC) problems. If your designs have suffered from these types of problems, you've probably looked for tools to help you predict and avoid such EMC difficulties.

What is EMC? The IEEE defines it as the ability of a device, equipment, or a system to function satisfactorily in its environment without introducing intolerable electromagnetic disturbances to anything in that environment.

Broadly speaking, when designing for EMC, you have to consider three major questions. First, is your system compatible with itself? Obviously, a system that jams or degrades its own performance is a problem. Signal-integrity problems usually fall into this group. Signal-integrity tools can help solve this problem.

Second, does your system introduce intolerable electromagnetic disturbances to anything in its environment? What constitutes "tolerable" varies from country to country, and standards organizations in the country where the system will operate define allowable limits. For example, in the United States, the FCC sets the requirements. In

Europe, the IEC has instituted a new set of strict EMC standards that will go into effect in 1996. Compliance testing is usually required on most systems to verify that a system doesn't violate the standards. Newly emerging EMC tools attack the emissions problem.

Third, does the surrounding environment adversely affect your system? If so, you have a susceptibility problem, which is typically more difficult to solve than are the other two types because it's difficult to know what the surrounding environment will be for every application. One of the reasons that standards organizations are developing emission standards is to specify an environment for which you can design. Specifying the maximum allowable emissions for a system can also tell you that another system in the vicinity will have emissions less than or equal to the maximum. Currently, none of the EMC-analysis tools effectively addresses the susceptibility problem.

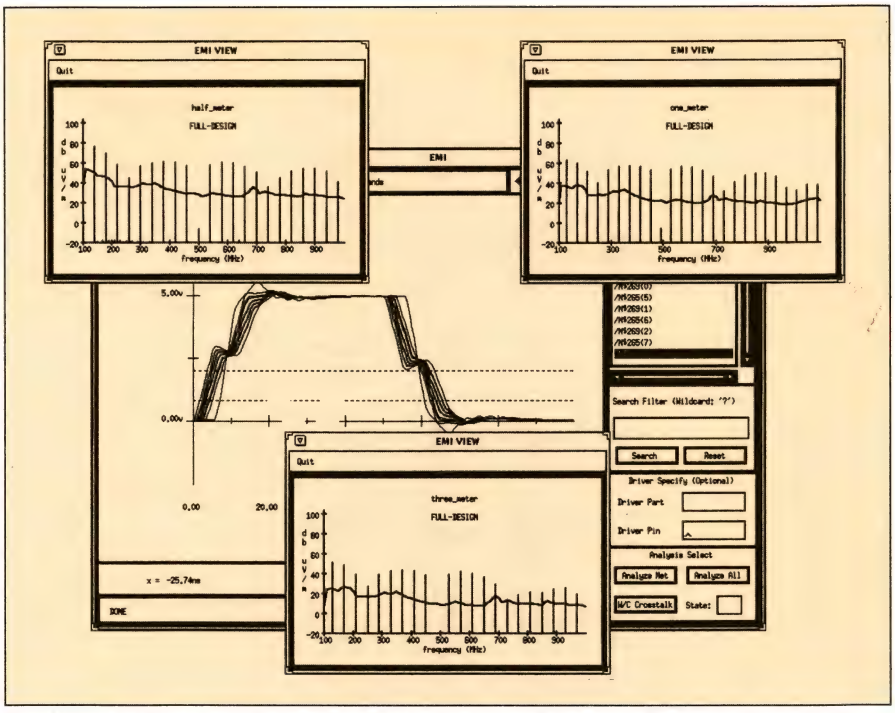
The methods of dealing with the first two EMC considerations differ, depending on which of the issues you are addressing.

The problems of an electronic system's compatibility with itself typically manifest themselves without any special testing when you attempt to operate the system. Signal-integrity tools help you at the design stage by predicting such problems before you build a system. This gives you a chance to change the design and avoid the problem.

Currently, the most common method of handling electromagnetic emissions is through compliance testing of the final product. Although emission testing is necessary and will remain so, finding EMC problems by testing a production system or prototype is undesirable. Product testing usually happens late in the development cycle, and problems may delay your product's completion date. The unit cost of the product may also increase because you typically don't have as many options available for correcting an EMC problem late in the development process.

To make their systems pass emission tests, engineers often try to seal a radiating mess inside a shielding enclosure. Although this technique is often necessary for passing emission testing, a well-designed system inside may reduce the cost of the enclosure.

Correcting an EMC problem earlier in the design stage may be as simple as moving components and traces around on a pc board. **Table 1** lists EMC-design tools that are or soon will be available. EMC tools that can help you at the design stage are of two types.



Quad Design's Quiet predicts EMI radiation at selected points in 3-D space for unenclosed pc boards and subassemblies.

Table 1—EMC-design tools

Manufacturer	Product	Price	Availability	Description
Ansoft	Maxwell SI Eminence	$49,900	March, 1994	Simulates emissions of multiple pc boards, cables, and enclosures
Aries Technology	MSC/ Aries EMC	$19,950 $950/month	Q1, 1994	Simulates emissions of multiple pc boards, cables, and enclosures
Contec	ContecRadia	$70,000	January 15, 1994	Simulates emissions from a pc board without an enclosure
Quad Design	Quiet	$60,000	Beta: Q1, 1994	Simulates emissions from a single pc board without an enclosure
Racal-Redac	EMC Advisor	$15,000	Now	Expert system evaluates compliance to EMC-design rules

Let an expert system help you

The first is an analysis tool that checks your adherence to rules that minimize EMC problems. As this article goes to press, the rule-based EMC tool called EMC Advisor is the only commercial tool that is actually available. EMC Advisor is a part of Racal-Redac's CAD Expert EDA-layout-design System but is an independent application. The tool is an expert system that evaluates a design to measure its relative compliance to a set of EMC-design rules. It is not a simulator, although you might want to use it as a complementary tool with an EMC simulator.

EMC Advisor evaluates a design against a set of 15 rules that focuses on the two categories of emissions: differential mode and common mode. Differ-

ential-mode emissions result from a current flowing around a loop, such as a signal and its return path. Common-mode emissions result from currents on the power-distribution system, such as transients in the ground plane. Poorly designed power-supply decoupling or improper component placement often results in common-mode emissions.

To evaluate a design, EMC Advisor analyzes layer stack, track shielding, impedance profiling, component placement, partitioning, power-supply decoupling, power-plane impedance, and power-plane overlap. You can also add your own rules. Because the tool uses data normally available in the design system, you can run the tool periodically as you perform a layout. Furthermore, you don't have to be an EMC expert to use EMC Advisor. After the tool completes its analysis, it highlights problem areas of the design in red and marginally problematic areas in amber. It also suggests improvements.

Although a rule-based EMC tool still leaves you guessing as to just what your systems electromagnetic emissions are, such a tool can effectively minimize potential EMC problems. For designers with limited knowledge of how to avoid EMC problems, the rule-based tools can help you create a better design that has a much better chance of passing emission tests without problems.

Even if you use an EMC simulator on the design, EMC Advisor may help you create a better design. Another advantage: EMC Advisor runs much faster than analysis tools that perform complete electromagnetic simulations.

Simulators help analyze your design

The second type of analysis tool for EMC design is a simulator. The benefit of simulators is well known: You get to see how your design behaves without actually building and testing the hardware. The major concerns with most simulators is how well they represent reality and how difficult it is to obtain or develop the models to use in the simulation. (See **box**, "The ABCs of EMC".)

The simulators in the **table** predict a system's frequency-dependent electric-field intensity at arbitrary points in space. The listed simulators simulate various types of systems.

For example, Ansoft's Maxwell SI Eminence simulates full 3-D systems, including multiple pc boards, cables, and enclosures. The simulators from Contec and Quad Design do not simulate the effects of enclosures. The EMC tools read physical-design data from a variety of compatible design tools. Make sure the tools you want to use are compatible with your physical-design tools. Such physical-design tools can include tools for pc-board layout, mechanical design, multichip-module (MCM) design, and IC-package design.

Ansoft's Maxwell SI Eminence uses a full-wave finite-element solver to solve the full, unsimplified Maxwell's equations in the frequency domain for characterization of arbitrary 3-D structures. The tool has an adaptive mesh-refinement capability to simplify mesh creation for the analysis of 3-D structures. The software is applicable to EMC and EMI problems in ICs, pc boards, cables, loops, cabinets, apertures, and radiating structures, such as microstrip, wire, slot, and horn antennas. The tool generates a Spice model of a system that runs on Spice simulators.

Aries Technology's EMC tool also analyzes 3-D designs using finite-element analysis. The software automatically generates the finite-element mesh from 3-D physical-design data. It predicts magnetic and electric fields and current densities, induced and applied voltages and currents, and power losses for frequencies from dc to RF. The analysis program provides results for any number of frequencies or in the time domain.

In June, Quantic Design will offer the EMC Greenfield EMC-analysis tool, but the company has not yet set a price for the product. The software models the radiated electromagnetic fields from multiple pc boards within an enclosure, including internal and external cables, using time- and frequency-domain analysis. The tool offers a choice of an approximate-but-fast solution or an exact analysis. Quantic will integrate EMC Greenfield with the company's other Greenfield transmission-line-analysis tools.

Contec's ContecRadia and Quad Design's Quiet model the radiated electromagnetic field of a pc board, MCM, or backplane with no enclosure. As the tools become commercially available, it will be interesting to watch Radia and Quiet. Although less ambitious than some of their competition, will they also

Manufacturers of EMC-design tools

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The ABCs of EMC

Zoltan Cendes, PhD, President, Ansoft Corp

Many designers may think of electromagnetic compatibility (EMC) as a black art and view its problems as mysterious, counterintuitive, or strange. Solutions to EMC problems tend to be heuristic, based on years of experience with trial-and-error methods. Yet, to understand EMC, you must first understand that the source of the phenomenon is electromagnetic. However, many designers find EMC confusing because they use inappropriate models or simple circuit models to represent complex electromagnetic phenomena.

Maxwell's equations govern electromagnetic fields. These equations predict that time-varying magnetic fields induce electric fields and that time-varying electric fields induce magnetic fields. At low speeds—with leading-edge rise times less than 1 nsec, for example—the induced fields are small, and you may overlook them. In these cases, using traditional lumped-circuit parameters, such as capacitance, inductance, and resistance, you can accurately model the voltages and currents in the components.

However, as computer speeds increase so that signals exhibit subnanosecond rise times, induced fields become significantly larger, and frequencies become higher. In these cases, ordinary circuit theory breaks down. As a result, there is no alternative to full-wave solutions—solving the full set of Maxwell's field equations.

A spiral inductor's field

The spiral inductor in **Fig 1** illustrates how a simple RLC model breaks down at high frequency. This spiral inductor has a three-to-one metalization pattern; that is, the conducting turns are three times as wide as the space between them. As a result, current is readily induced in neighboring turns. A low-frequency solution, assuming the absence of induced currents in the conductors, provides a lumped-parameter response that rises monotonically with frequency (see the green line in **Fig 2**). Measuring the circuit and providing a full-wave solution of Maxwell's equations determines the actual circuit behavior. This is a much more complicated solution (see the red and blue lines in **Fig 2**).

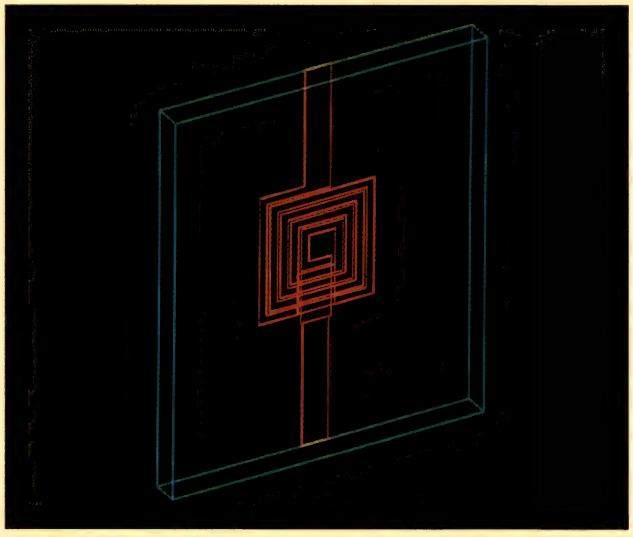

Fig 1—This spiral inductor operates like a classical dipole loop antenna.

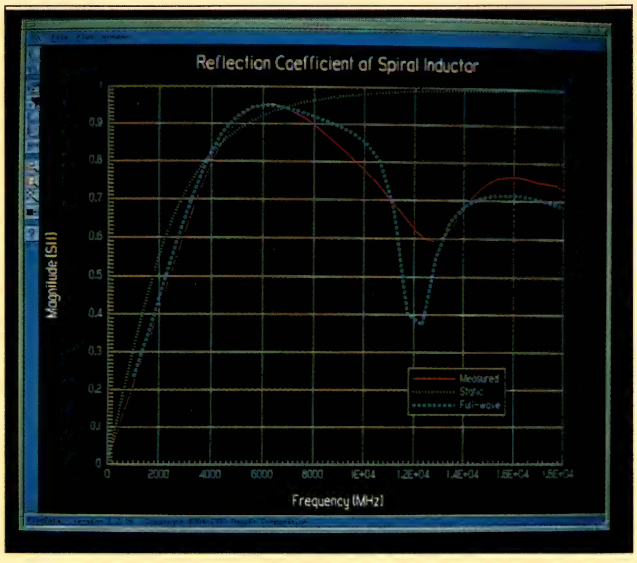

Fig 2—The green line shows the low-frequency analysis of the inductor in Fig 1, ignoring the induced currents. The blue line shows the full-wave solution of Maxwell's equations, and the red line shows the measured response.

In this case, the low-frequency model is accurate to about 5 GHz but breaks down at higher frequencies. Clearly, the low-frequency, lumped-parameter circuit model is useless at high frequencies. Although 5 GHz appears to be a very high frequency, it may not be. For example, a digital circuit operating with a 1-nsec rise time has a significant amount of leading-edge harmonics at this frequency.

What is going on here? Why does the performance of the spiral inductor depart so radically above 5 GHz from the behavior that circuit theory predicts? There are three reasons.

First, as the frequency rises, the current no longer flows in the familiar stream-function patterns common to low frequency. Instead, the current crowds toward the edges of the conductors due to skin effect.

Second, eddy currents are induced in the ground plane below the spiral. These ground-plane eddy currents further alter the inductance and resistance values of the inductor.

Third and most important, high-frequency electronic components set up and radiate electromagnetic waves. These waves establish resonances and standing wave patterns in the inductor, dramatically altering the voltage and current patterns and radiating energy away from the system. In fact, at high frequency, the spiral inductor in **Fig 1** operates like and exhibits behavior similar to that of a classical dipole loop antenna. Because the radiation from a loop antenna grows with the square of the frequency, inductor performance deteriorates rapidly following the onset of radiation.

Fig 3 shows the far-field radiation pattern for the spiral

inductor at 10 GHz. At this frequency, 10 to 15% of the energy input to the inductor radiates away.

Solving EMC problems, therefore, involves determining the underlying electromagnetic fields. For low frequencies, you can solve the quasistatic field equations for LCR, and you can use the resulting values and quasi-transverse-electromagnetic analysis to simulate signal-integrity phenomena, such as crosstalk, ringing, and ground bounce. At midrange frequencies, you must model the eddy currents in the conductors by solving the electromagnetic-diffusion equation.

However, at leading-edge rates lower than 0.1 nsec, there is no alternative to solving the full set of Maxwell's equations. The full-wave solution is difficult to compute. However, once you compute it, you can generate a full-wave Spice model to interface directly with circuit simulators.

Fortunately, finite-element methods to compute full-wave solutions have emerged in recent years. In many cases, these methods provide easy and highly accurate solutions to EMC problems. Consider, for example, the layout of the pc-board power and ground traces in **Fig 4a**. Ansoft's Maxwell SI Eminence simulated the layout.

The first step in simulating the radiated emissions is to enter the geometry of the structure by using the software's solids-modeling system or by reading the geometry from a CAD file, such as GDSII, Gerber, or AutoCAD. Next, define the materials in the structure and the input signals. Finally, the software creates and refines the finite-element mesh, solves the resulting matrix equations, and determines the frequency response.

After the software completes the solution, you can test the solution in many ways, including having the software compute inductance and reactance as a function of frequency, determine resonances and standing wave patterns, and plot near- and far-field patterns. **Fig 4a** shows a plot from the pc board of the near field at 100 GHz. The plot shows that placing the power and ground leads on opposite ends of the pc board creates a large current loop that emits excessive radiation.

To dramatically reduce the radiated emissions from the pc board, the designer rerouted the ground trace to lie directly under the power trace. **Fig 4b** shows the resulting near field at 100 GHz.

Thus, solving EMC problems is not a black art after all. The electromagnetic fields in electronic components causes these problems. Using full-wave finite-element methods to solve these fields directly, you can perform a precise simulation of EMC phenomena and minimize electromagnetic coupling and emissions.

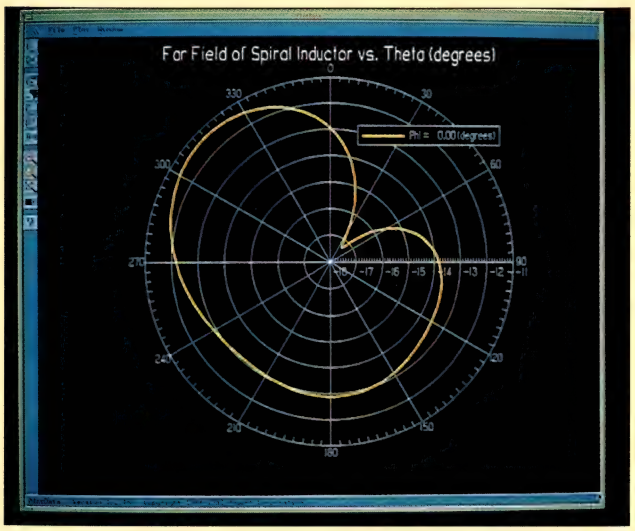

Fig 3—The radiation pattern of Fig 1's spiral inductor at 10 GHz shows that 10 to 15% of the energy input to the inductor radiates away.

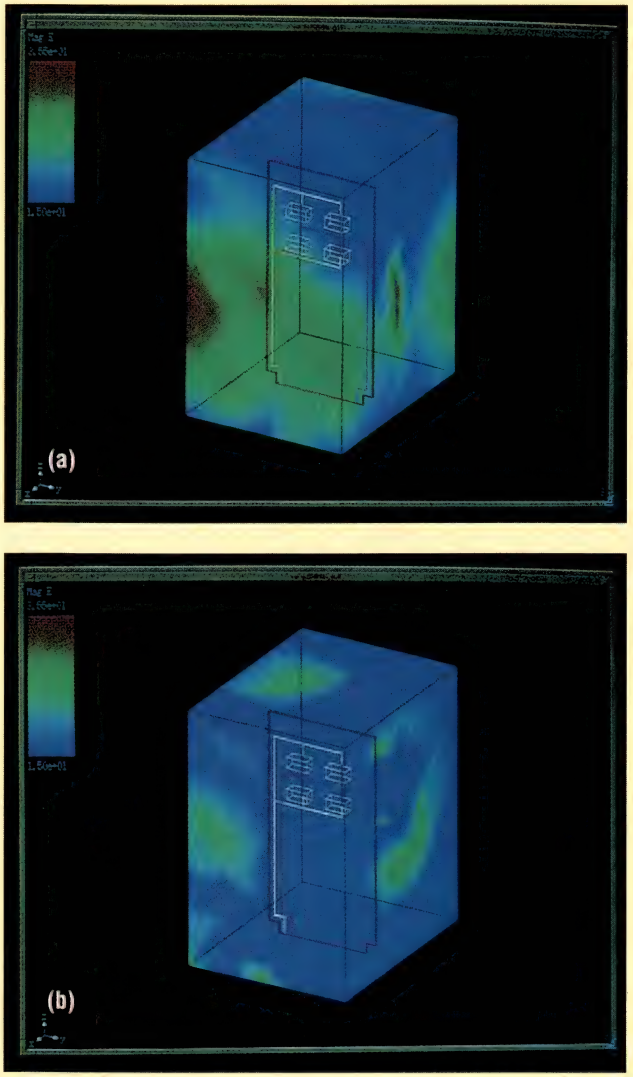

Fig 4—A plot from the pc board of the near field at 100 GHz shows that placing the power and ground leads at opposite ends of the pc board creates a large current loop that emits excessive radiation (a), indicated by red. Reducing the loop area (b) of the power and ground trace significantly reduces the radiated energy.

EMC-DESIGN TOOLS

prove to be less capable, or more realistic for real-world problems?

ContecRadia calculates radiated-noise and electric-field intensities, including electrical effects, reflection, and crosstalk of transmission lines in high-speed, high-frequency digital, analog, and mixed-signal systems. After extracting the electrical models from layout files, the ContecSpice circuit simulator calculates time-domain current and voltage distributions in the conductor traces. It uses the current distribution on the conductive traces to calculate the radiated electric-field intensities, based on loop-antenna principles.

Quad Design's Quiet uses transmission-line simulation to model the network waveforms and then sums the radiation from each net segment to get the radiation from the entire net relative to one or more specified points in space (the receiving antenna location). By summing the radiation from all nets, the software obtains the full board radiation.

Quiet simulates networks in the time domain using linear and nonlinear driver, receiver, and terminator characteristics. By accurately modeling the network-signal characteristics of all modern logic families, the software can accurately model the radiated energy. The software lets you specify the characteristics of each signal on every net or just the clock frequencies. It also lets you use pseudorandom signals to simplify the definition of signal activity.

Although the Radia and Quiet simulators handle only pc boards and do not include the effects of an enclosure, don't count them out as useful tools to help you stay out of EMC problems. The shielding effects of a conductive enclosure are useful and often necessary, but reducing radiated energy at its source is usually best.

An analysis tool that lets you work on a single board at a time can help you maintain low emission levels. However, such a tool does not let you obtain accurate data on the radiated energy of the entire system outside its enclosure—something you may want to know if you anticipate problems when you run emissions tests on the completed system.

Also, remember: Tools that help reduce transmission-line and signal-integrity problems typically result in lower emission levels.

Kellee Crisafulli, president of HyperLynx, a manufacturer of signal-integrity-analysis tools, reports that some of the company's customers find that when they clean up their transmission lines, they also reduce EMI and RFI.

The future for EMC-analysis tools for radiated emissions looks promising and competitive. Many of the companies that offer transmission-line-analysis tools expect to have EMC tools available within the next year. With the ever-increasing clock rates of many electronic systems, EMC is likely to become a more familiar acronym. EDN

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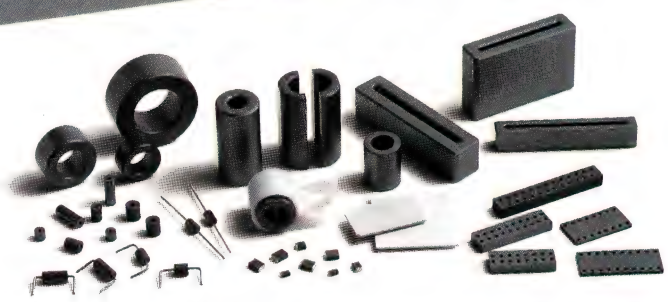

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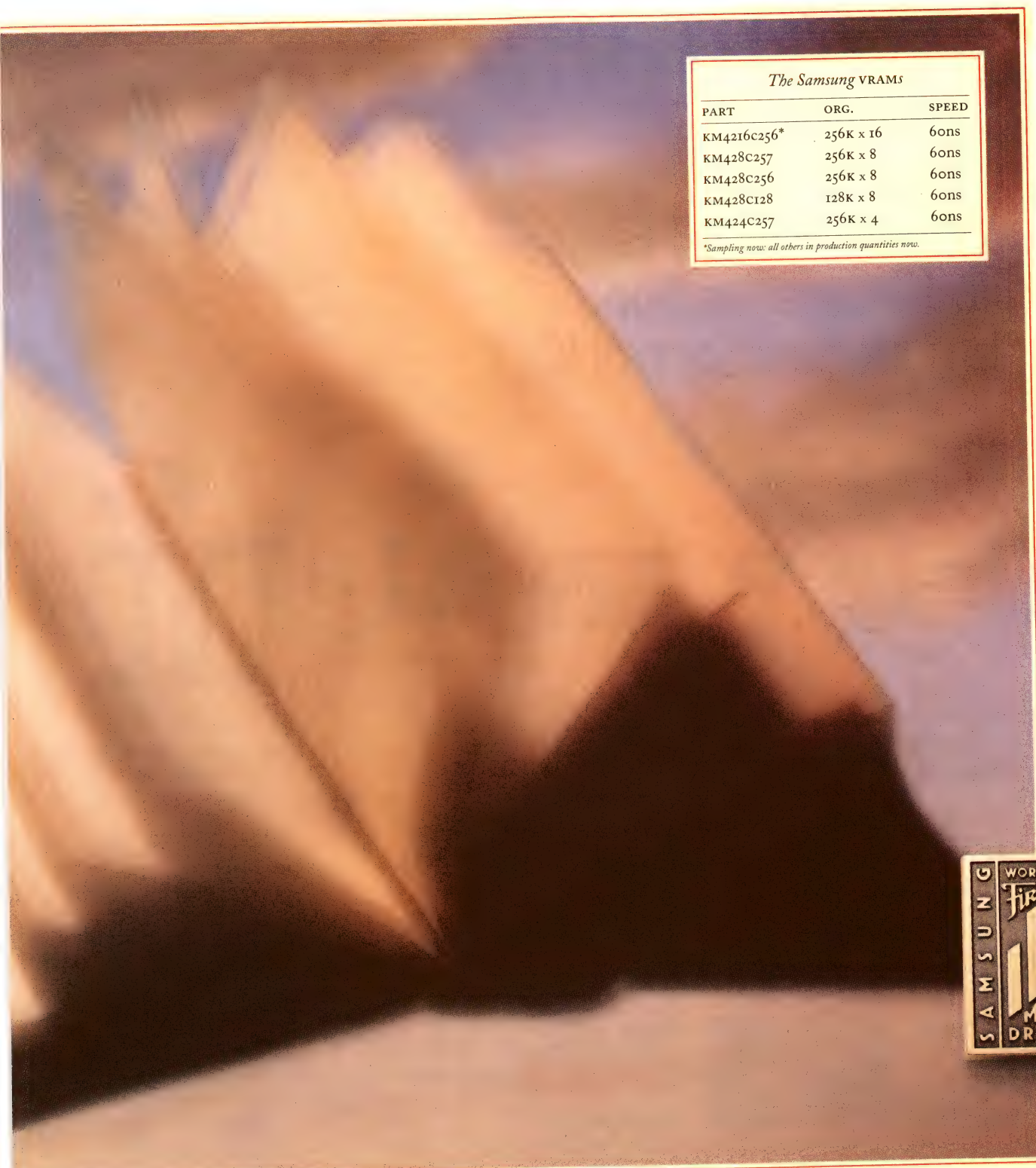

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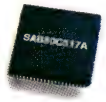

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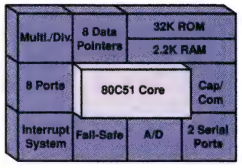

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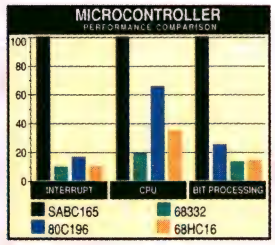

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PLD-design methods migrate existing designs to high-capacity devices

Mike Trapp, Lattice Semiconductor Corp

Moving to newer higher capacity programmable devices can give you higher density and better performance. But if you use common CAE design tools, transferring your old design's description to the new device's development environment may be difficult. PLD-design methods help ensure that your design remains transportable.

All CAE tools accept PLD-design methods. Thus, using PLD-design methods leads to a very simple method for moving designs to new types of PLDs. Using these methods helps you take advantage of the increased performance and lower cost of newer devices and lets you combine new designs with existing ones.

Overcoming proprietary databases

Each CAE vendor has developed a proprietary database for sharing circuit-design information among its own tool set. To transfer circuit-design information from one vendor's tool set to another's, you must perform a complex translation. This translation may misinterpret or drop information altogether, yielding an erroneous result.

The ostensible "industry-standard" Electronic Design Interchange Format (EDIF) netlist typifies this problem. EDIF can represent circuits at levels ranging from a complete graphical, functional, and parametric representation to only a primitive functional representation. As a result, one vendor's EDIF netlist reader may not totally understand another's EDIF netlist. Consequently, using incompatible netlists would make your translation at least incomplete and at worst inaccurate.

However, translation becomes simple and reliable if you use PLD-design methods to express your design. In particular, most designers use Boolean equations to describe their PLDs' functions because of the AND/OR architecture of PLDs. Fortunately, because PLDs have become extremely popular as a "can-do-anything" circuit element, CAE vendors have integrated PLD-development tools into their CAE tools. These tools produce Boolean equations in various formats, which you can easily translate from one to another, giving an accurate and complete functional description of a circuit.

To illustrate, consider the high-level description of a 10-bit, up/down, preloadable counter in **Listing 1** (see *EDN* BBS). This functional description uses ABEL 4.XX, a device-independent language. A device's description at this level does not translate easily to any specific PLD. However, you can use a PLD compiler to transform the

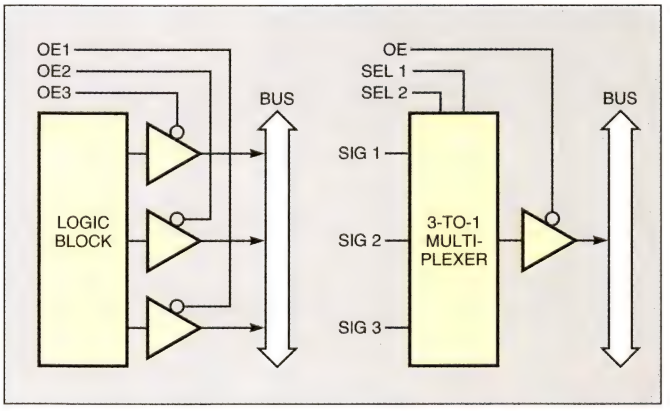


Fig 1—You can translate 3-state buses into 1-of-N selection functions for implementing in a high-density programmable device.

BBS

The software listings in this article are available on EDN's computer bulletin-board system (BBS). Phone (617) 558-4241 with modem settings 300/1200/2400 8,N,1. Access */freeware* SIG and specify *(r)ead* option followed by *(k)eyword* search for "MS #533."

PLD-DESIGN METHODS

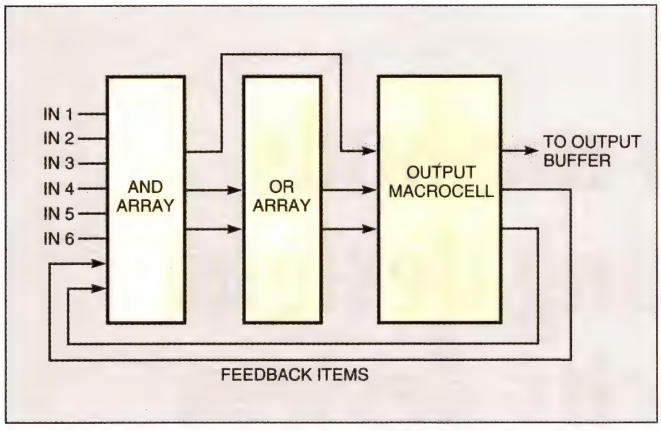


Fig 2—Boolean expansion may improve device utilization but can introduce feedback terms.

high-level ABEL description into reduced Boolean equations (**Listing 2** on *EDN* BBS)—the fundamental description of a 10-bit up/down counter. Now, you can move this Boolean representation of the counter to virtually any development environment with only minor changes.

Because all mainstream PLD compilers produce reduced equations with virtually identical syntax, migrating these equations from tool to tool is simple. For instance, the PDS tool from Lattice for developing devices in the company's pLSI family has an equation syntax virtually identical to ABEL's reduced-equations syntax. Similarly, the PLA files that ABEL, Minc, and CUPL produce all follow the standard rules for PLA-file syntax.

You can even extend this technique of obtaining reduced, transferable equations from a schematic diagram. Many CAE companies include PLD compilers, with associated PLD libraries, in their design environments. With components from their PLD library, you can use the CAE tools to produce reduced Boolean equations that describe the schematic. You can then integrate these equations with functions expressed in a PLD-description language to form a set of equations that completely describes your circuit. The design tools may produce these equations in the familiar textual form or in an industry-standard format known as PLA (see **box,** "Interpreting PLA files").

If you capture your old designs in the form of these equations, you just follow a series of basic steps to implement them in a new programmable device:

- Define the I/Os.

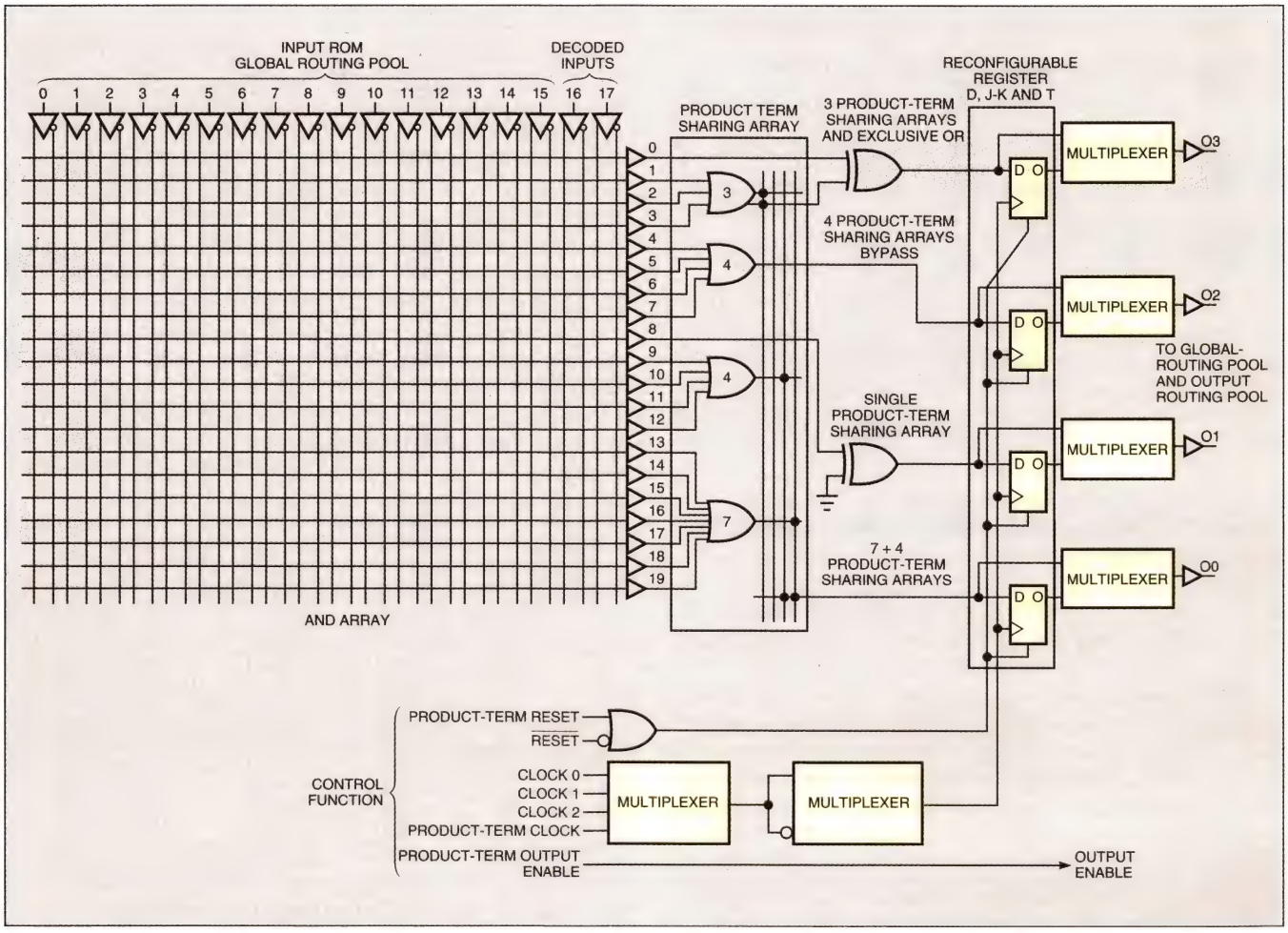
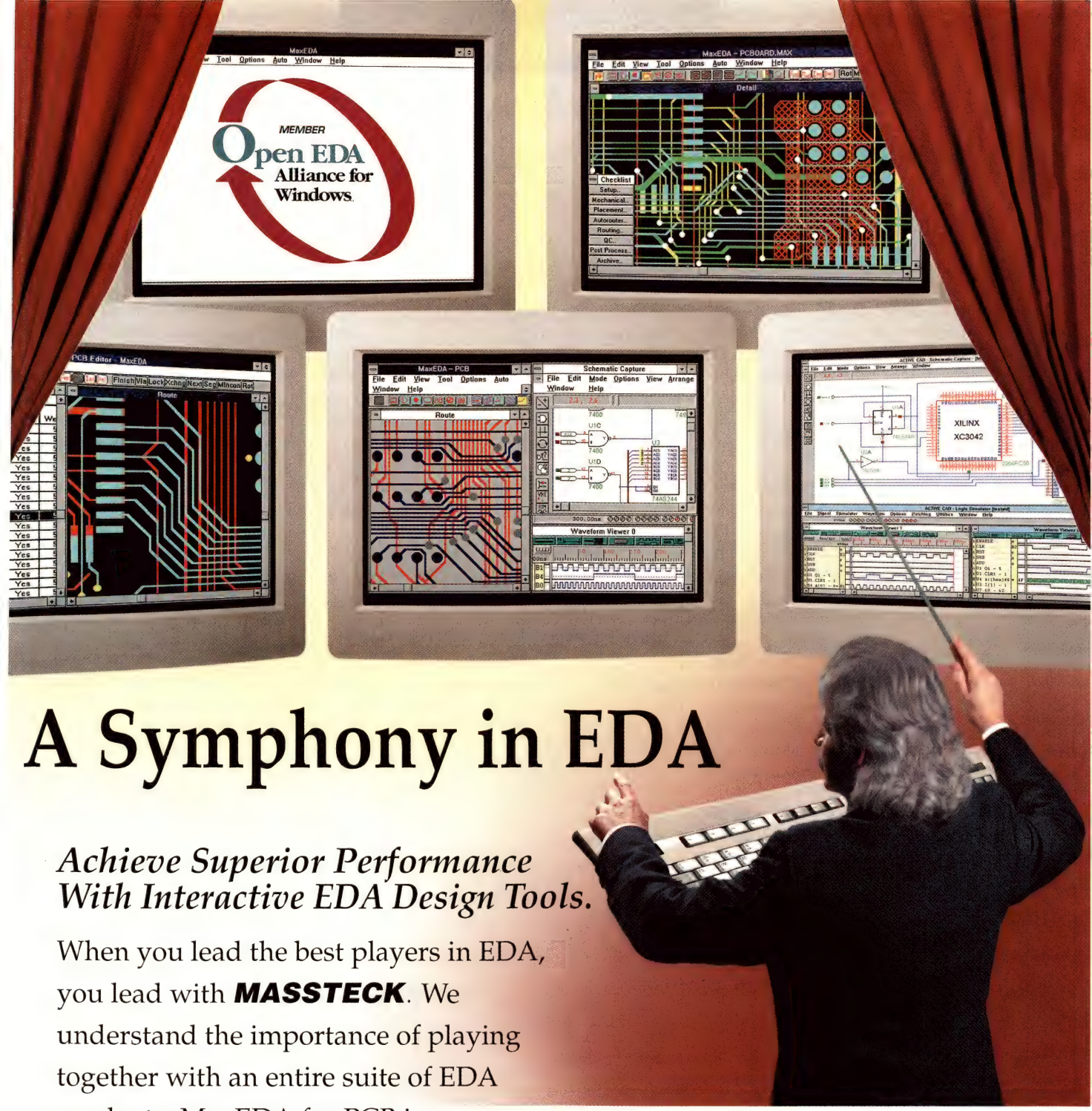


Fig 3—The pLSI logic block allows different product-term-sharing combinations for implementing various logic functions.



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CIRCLE NO. 88

Interpreting PLA files

Listing A shows the PLA-format file for the 10-bit up/down counter. The statements preceded by #$ indicate that information is not necessary to the circuit description but may be used by post processors such as fitters. An example is the #$ PIN statement, which is an I/O list of all signals entering and exiting the device and may even indicate a specified PIN number. The plus (or minus) symbol following the pin name indicates that the register node has a buffer or inverted between the register and the output pin. Polarity designators have no meaning for inputs or combinatorial outputs.

The .i and .o statements indicate the number of inputs and outputs, respectively. The number of inputs includes nodes feeding back as circuit inputs. The number of outputs includes actual combinatorial signal outputs and signal outputs controlling the D input, the D asynchronous set, and the output-enable equations.

The .type f statement indicates the format of the PLA file. The F format shows equations implemented in only positive logic, and the alternative FR format shows the equations implemented in both positive and negative logic.

The .ilb and .ob statements identify inputs and outputs, respectively, of the PLA file. Feedback nodes included as inputs have an .FB extension. The outputs also use dot extensions to indicate that the output signal is registered (.REG) or part of an exclusive-or equation (.X1 and .X2).

The .phase statement indicates if the signal should be complemented (.phase 0) or not complemented (.phase 1). The .p indicates the number of product terms required to define the circuit's function. The table following the .p statement defines the product terms.

The table has two sections. The first section defines the inputs to the product term and has a column for every input defined. A minus sign in a row indicates the input for that column is a "don't care" for that product term. A one or a zero in a column indicates that the product is true when that input is a one or a zero, respectively.

The output section reads similarly. This section has a column for every output defined. A one in a column indicates that the product term defined in the input section is a product term required for that output.

Following these rules, you would interpret the equations for Q9.REG as follows (Q9.FB is the first output defined in the .ob section): When loadl is complement, and D9 and clr are true, the product term becomes the output Q9.REG. When loadl, clr, ce, and Q9.FB are true, the product term becomes the output Q9.FBn. And so on...

This file looks very cryptic, but it is actually a very compact way to describe large complex circuits. The PLA format is an industry standard; hence, tools that use it as input can interface with tools that produce PLA file as output.

Listing A—PLA-format file

```
#$ TOOL ABEL 4.10
#$ DATE Mon Oct 5 14:41:38 1992
#$ TITLE 10 bit up down loadable counter
#$ TITLE Michael Trapp Lattice Semiconductor  Oct 1990
#$ MODULE _10bitctr
#$ JEDECFILE count10
#$ VECTORFILE _10bitct.tmv
#$ PINS 26 Osc OE Q9+ Q8+ Q7+ Q6+ Q5+ Q4+ Q3+ Q2+ Q1+ Q0+ loadl D9 D8 D7 D6 D5
  D4 D3 D2 D1 D0 u_d ce clr
.i 26
.o 30
.type f
.ilb Osc OE loadl D9 D8 D7 D6 D5 D4 D3 D2 D1 D0 u_d ce clr Q9.FB Q8.FB Q7.FB
  Q6.FB Q5.FB Q4.FB Q3.FB Q2.FB Q1.FB Q0.FB
  ob Q9.REG Q8.REG Q7.REG Q6.REG Q5.REG Q4.REG Q3.REG Q2.REG Q1.REG
  Q0.REG Q9.C
  Q8.C Q7.C Q6.C Q5.C Q4.C Q3.C Q2.C Q1.C Q0.C Q9.OE Q8.OE Q7.OE Q6.OE Q5.OE
  Q4.OE Q3.OE Q2.OE Q1.OE Q0.OE
.phase 11111111111111111111111111111111
.p 131
—01————————1———————— 10000000000000000000000000000000
—1————————-111———————— 10000000000000000000000000000000
—1————————0010000000000 10000000000000000000000000000000
—1————————0-11————————1 10000000000000000000000000000000
—1————————0-11————————1- 10000000000000000000000000000000
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—1————————1-1————————10 00000000100000000000000000000000
—1————————101————————01 00000000100000000000000000000000
—0————————1—1———————— 00000000100000000000000000000000
—1————————-11————————-1 00000000100000000000000000000000
—1————————-01————————-0 00000000100000000000000000000000
1————————————————————- 00000000001111111110000000000
-0———————————————————— 00000000000000000001111111111
.e
```

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CIRCLE NO. 114

PLD-DESIGN METHODS

- Compile and minimize PLD equations.
- Add MSI and SSI functions.
- Implement 3-state circuits, inversions, and preset/reset.
- Combine all PLD source files into a single file.
- Partition the circuit over the new device's logic blocks.
- Import and verify the design.
- Place and route the design using tools for high-density devices.
- Assign the I/O pins.

An upgraded PLD design begins with defining the I/Os of the new device based on the circuit developed for the old devices. You must first determine if the new design will be pad-limited (the new device does not have enough I/O pins) or gate-limited (the new device does not have enough internal logic).

If the design is pad-limited, you must choose a device with a higher pin count or partition the design among two or more lower-pin-count devices. Using a higher-pin-count device raises the cost of the implementation and typically results in a large amount of unused internal logic. Multiple lower density devices typically incur a lower cost and better utilization of available logic.

A gate-limited design mandates that you select a higher density device. This choice usually leads to unused I/O pins. You can take advantage of the unused pins to introduce additional functions, providing that the design does not become gate-limited again.

A shotgun approach

As a shotgun approach, you can simply draw a box around a circuit, count the I/O and gate requirements, and select a programmable device meeting this gate and I/O count. However this simple-seeming task can be complex, requiring good engineering judgment of how to best use the high-density device.

Another straightforward method to estimate gate count uses SSI, MSI, and PLD equivalents. By adding the number of these circuit blocks required for a circuit, you can determine if the design fits into a high-density device. For instance, the generic logic block of the pLSI family of high-density devices is roughly equivalent to one-half of a 20V8 PAL device. Extending this approximation, roughly one MSI device or two SSI devices can fit into each logic block.

To partition a circuit implemented with MSI, SSI, and PLDs, look for those nodes that are best suited for interconnection within the new device. These nodes typically travel from one device to only one or two other devices. Assign nodes that connect to many devices to the new device's I/O pins, unless you vacuum all the destination devices into the new high-density device.

This approach eases determining whether you should implement a node within the high-density device or allocate it as an I/O pin. Signals that connect to a device not implemented in the high-density device become I/O pins by default. Naturally, nodes going off-board must become I/O pins of the high-density device.

Clocking affects partitioning

Clocking can also impact how you partition a circuit. If the circuit requires more clocks than are available in one of the new devices, for example, you should partition the circuit over multiple devices, such that circuits with common clocks are in the same device.

After defining the circuitry to be placed into the new device, you begin converting the design into the new device's format. A typical design contains many PLDs and a few MSI and SSI devices. Most PLDs have an associated source-equation file, the source for design equations to be imported into the device-specific software for the new high-density device.

You should reminimize the old equations in the original PLD design before converting them into the high-density device's format. While designing with PLDs, you typically use only Boolean reduction. Advanced reduction algorithms available with standard third-party compilers can further reduce the number of product terms required for a function. These reductions produce a lower gate count and easier implementation into the high-density device.

In some cases, the original design's documentation may not be available. In such a case, you may have only to access a JEDEC fuse map for some PLDs. You must decompile this fuse map into the source equations and reminimize the equations. The decompilers produce raw equations that have generic names for the equation's variables and parameters:

```
Pin23 := Pin01 & Pin02
 # Pin03 & Pin04 & Pin05 .....
 # Pin09 & Pin10;
Pin23.OE= Pin06;
```

Although functionally correct, these equations are difficult to read. Using the "search-and-replace" function available on word processors, you can recast the generic signal names to match those on your schematic. Signal naming is important because development software and high-density development software connect signals with common names.

Add MSI and SSI functions

At this point, you should add any MSI and SSI functions that you want in your revised design. You can easily integrate MSI and SSI functions into the new device by creating a PLD-design file that emulates the functions and importing that file into the device's design software. Most MSI functions fit neatly into a PLD, especially when a designer uses a PLD such as a 22V10 PAL device whose flexible architecture simplifies I/O and product-term allocating. The same procedure for SSI devices is applicable, but combining AND, OR, and INVERTERS into the MSI- or PLD-design equations should be very simple.

By using the same names on the inputs and outputs of the MSI PLD as on the schematic, the resulting file becomes ready for converting and importing.

An alternative method for implementing these functions is to find the closest equivalent circuit to the desired function within the macro library provided with the high-density-device software. Both of these techniques aim to develop functionally correct equations that best utilize the pLSI's architecture.

You can then add PLD files containing MSI and SSI func-

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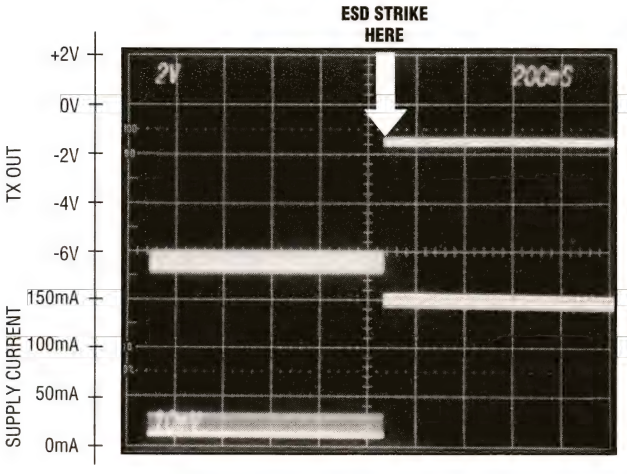
TYPICAL BIPOLAR LATCHED BY -2kV TO -10kV ESD



Bipolar Charge Pump Output can collapse, and supply current can increase to 150mA when the receiver input is zapped with -2kV to -10kV, latching the device.

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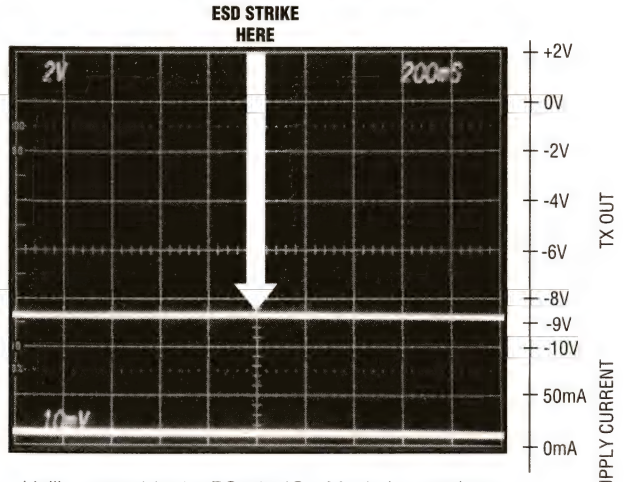

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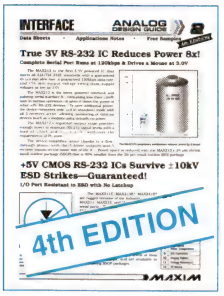
MAX213E	4/5	±10kV	0.1	Yes	120	2	15µA	$3.62
MAX241E	4/5	±10kV	1.0	Yes	120		1µA	$3.62

**ESD testing done on all RX in and TX out pins using Human Body Model waveform detailed in Mil Standard 883 method 3015.7
†1000 up, suggested resale FOB USA.



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CIRCLE NO. 91

PLD-DESIGN METHODS

tions to the files containing the converted PLD equations. The goal is to derive functionally correct equations in standard compiler format.

Convert 3-state signals to multiplexers

Trying to implement 3-state buses within an ASIC or high-density devices can create problems, such as causing outputs to go undefined. In fact, many high-density devices can't implement internal 3-state buses at all. As a solution, you can implement 3-state functions with a 1-of-N select function (**Ref 1**). The inputs to the selector are the signals that would be tied together on the 3-state bus. The select lines of the selector are the individual 3-state enable signals. This technique, commonly used in ASICs, appears in **Fig 1**.

You would rewrite the 3-state equations for a 1-of-N selector this way:

```
BUSA_SIG1=SIG_1A
BUSA_SIG1.OE=SIG1_OE
BUSB_SIG1=SIG_1B
BUSB_SIG1.OE=SIG1_OE

BUSA_SIG2=SIG_2A
BUSA_SIG2.OE=SIG2_OE
BUSB_SIG2=SIG_2B
BUSB_SIG2.OE=SIG2_OE

BUSA_SIG3=SIG_3A
BUSA_SIG3.OE=SIG3_OE
BUSB_SIG3=SIG_3B
BUSB_SIG.OE=SIG3.OE

 BUSA_OUT= (!SIG1_OE & !SIG2_OE) & SIG_1A
  # ( SIG1_OE & !SIG2_OE) & SIG_2A
  # ( SIG1_OE & SIG2_OE) & SIG_3A;

 BUSB_OUT= (!SIG1_OE & !SIG2_OE) & SIG_1B
  # ( SIG1_OE & !SIG2_OE) & SIG_2B
  # ( SIG1_OE & SIG2_OE) & SIG_3B;
```

The six original equations now appear as the two functions of BUSA_OUT and BUSB_OUT. Note that you do not need SIG3_OE.

Assuming that the SIG_1A and SIG_2A expressions use typical PAL-type equations, they would have this AND/OR structure:

```
SIG_1A= SIGA1 & SIGA2 & SIGA3
 # SIGA4 & SIGA5 & SIGA6;
SIG_2A= SIGB1 & SIGB2 & SIGB3
 # SIGB4 & SIGB5 & SIGB6
```

Then the selector equation becomes

```
BUSA_OUT= (!SIG1_OE & !SIG1_OE) & SIG1 & SIG2 & SIG3
 # (!SIG1_OE & !SIG1_OE) & SIG4  & SIG5  & SIG6
 # ( SIG1_OE & !SIG2_OE) & SIGB1 & SIGB2 & SIGB3
 # ( SIG1_OE & !SIG2_OE) & SIGB4 & SIGB5 & SIGB6
 # ( SIG1_OE &  SIG2_OE) & SIG_3A;
```

The AND function on the output enables (SIG1_OE, SIG2_OE) does not increase the number of product terms required to implement the various bus-signal functions. This result holds true for product-term-oriented architectures, such as the pLSI devices.

Investigate inversions

Given the wide variety of device architectures, you should investigate active-high vs active-low internal signals to achieve the highest utilization of the device's resources. The following equation is an example:

```
!OUT= IN1 & IN2 & IN3 # IN4 & IN5 & IN6;
```

If you can't implement this equation with a hardware inverter, you can use Boolean expansion to produce an alternative:

```
OUT=!IN1 # !IN2 # !IN3 & !IN4 # !IN5 # !IN6;
```

This equation requires seven product terms as opposed to two when implemented into a PLD-type device architecture like that in the pLSI devices (**Fig 2**). The expanded Boolean equation also requires two extra feedback terms to implement the OR-AND function in an AND-OR device architecture.

Define preset/reset mechanism

A frequently neglected, but nonetheless necessary, requirement for digital designs is a reset mechanism. All state-machine designs should have a known power-up state. If you attach a reset line to all your state-machine registers, such a line would unnecessarily use significant routing resources. The reset mechanism should take advantage of the hardware-reset resources available in the new device. You should remove individual reset signals from your design equations and instead use hardware reset.

Many programmable-device architectures provide only reset and no preset mechanism. In these cases, you can complement outputs requiring a preset signal and still use the hardware reset. Alternatively, you can make the preset function synchronous by adding a preset term into the design's equations.

Last, when placing new logic in the high-density device, you should partition that logic into available logic resources. For the pLSI family, you simply write Boolean equations or use the available macros. With the exception of a few keywords, you can enter the equations just as you would using third-party design tools.

Combining source files and partitioning

The *.DOC files produced by third-party compilers come in an industry-standard format. These files contain reduced equations derived from the source file, JEDEC maps, high-level state-machine language, truth tables, and standard equations. You should combine all the individual PLD and MSI *.DOC files into a single source file for partitioning over the high-density device.

Using a pLSI device as an example, you can collect equations into groups of four outputs to partition the PLD equations to fit into the four outputs of the pLSI device's logic blocks (**Fig 5**). (You must place headers and trailers around the four equations to direct the pLSI design software to partition the equations into a particular logic block.)

The software then maps the equations into the logic block's 18 inputs, 20 product terms, and four registered or combinatorial outputs. Additional logic capacity results from product-term sharing among the four outputs and an optional exclusive-OR gate fed by a product term and an AND-OR term.

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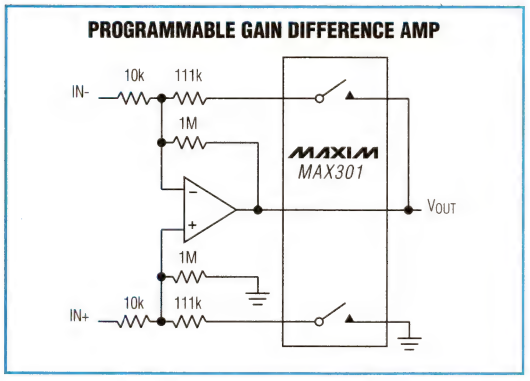

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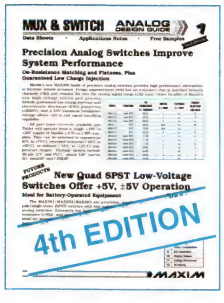
MAX303	dual SPST	30	2	3	15	✔	2.57
MAX305	dual SPST	30	2	3	15	✔	2.57
MAX317	SPST	30	N/A	3	10	✔	1.05
MAX318	SPST	30	N/A	3	10	✔	1.05
MAX319	SPST	30	2	3	10	✔	1.41
MAX333A	quad SPST	30	2	3	10	N/A	3.60
MAX351	quad SPST	30	2	3	10	✔	1.76
MAX352	quad SPST	30	2	3	10	✔	1.76
MAX353	quad SPST	30	2	3	10	✔	1.76
MAX361	quad SPST	85	2	9	10	✔	1.29
MAX362	quad SPST	85	2	9	10	✔	1.29
MAX364	quad SPST	85	2	9	10	N/A	1.14
MAX365	quad SPST	85	2	9	10	N/A	1.14



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CIRCLE NO. 92

PLD-DESIGN METHODS

The final conversion step is defining the I/O cells. The I/O cell for the pLSI device's definition is

```
SYM IOC IOXX 1;
XPIN XSIGNAME PIN# LOCK#;
IB1/OB1 (SIGNAMEIN/SIGNAMEOUT,SIGNAMEIN/SIGNAMEOUT);
END;
```

(Because the pLSI software routes the pLSI devices according to signal name, it automatically connects all I/O cells to the proper internal nodes.)

Import, verify, and lay out the design

Once you have partitioned your design over the new device(s), you must import the device's source file into the design software for verifying, placing, and routing. You then follow the steps outlined for the device's development environment.

This technique for creating a design for a programmable device builds upon PLD-design methods. In summary, the following guidelines can simplify your efforts:

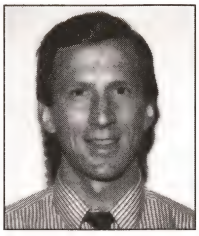
- Decide if the design is I/O- or gate-limited.
- Choose the appropriate new device.
- Use as many of the original Boolean functions from low-density source files as possible.
- Convert 3-state outputs to 1-of-N multiplexer outputs.
- For reset functions, use the global reset for the entire device or asynchronous reset for specific logic resources.
- Remain within the logic resources when partitioning the circuit.

Following this method brings you the significant manufacturing benefits of new generations of programmable devices: smaller boards, simpler test procedures, faster development, and fewer parts in inventory and assembly. EDN

Reference

1. Small, Charles H, "Where CMOS rules, multiplexers slave," *EDN*, August 5, 1993, pg 57.

Author's biography



Mike Trapp is a field applications engineer for Lattice Semiconductor in Irvine, CA. He has worked at his present job for three and one-half years. He obtained a BSEE form the University of Colorado, Boulder. In his spare time, he enjoys soccer and other outdoor sports.

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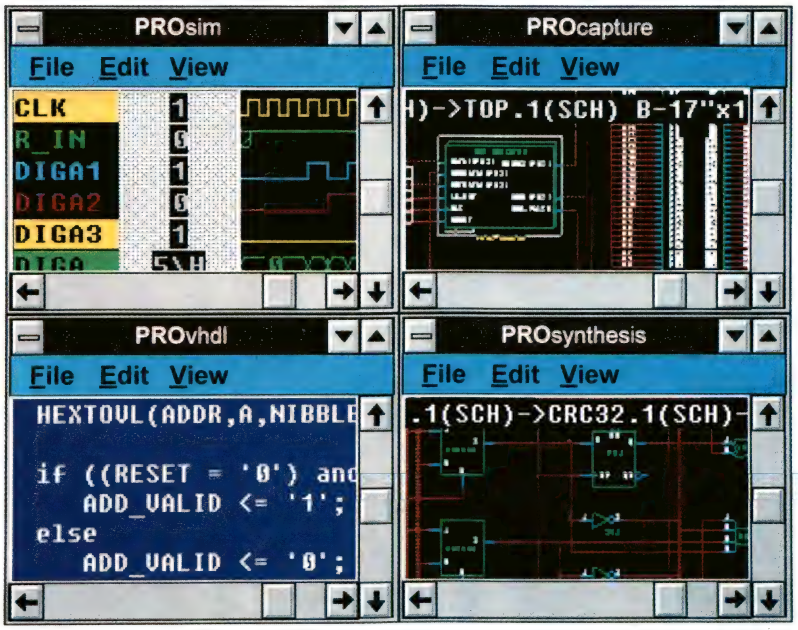

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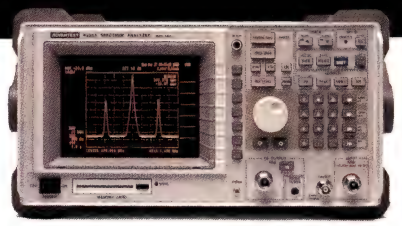

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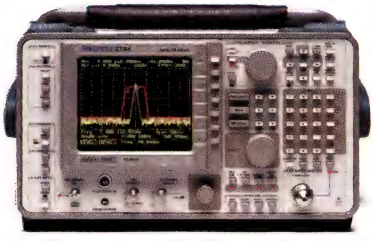

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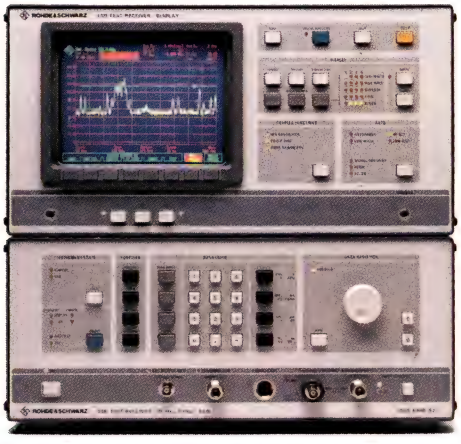

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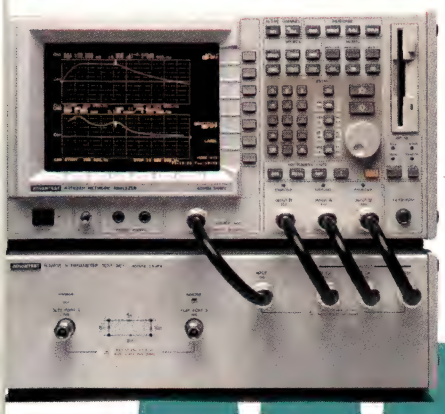

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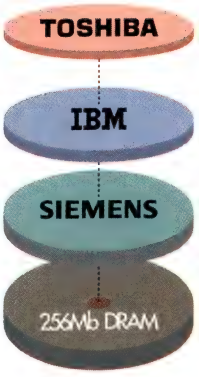

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CIRCLE NO. 81

Quantify critical-timing risks with statistical analysis

James J Vorgert, Texas Instruments Inc

Performing a timing analysis using conservative worst-case methods may force you to over design or reduce performance goals unnecessarily. Using statistical methods to quantify the risks associated with critical timing paths lets you trade off technology vs performance and manufacturing goals.

Timing is critical for a digital system's success. For decades, designers have analyzed circuits' timing using conservative worst-case methods. Such methods ensure reliable systems, but many are overly conservative. They also provide little insight into the risk of retaining a signal path that analysis shows exceeds its timing requirements. Statistical timing analysis can quantify the risk associated with that signal path.

Formally stated, a signal path is "a series of interconnected nodes in a digital design that are defined to begin and end with a constrained device or pin" (**Ref 1**). Most digital designs have thousands of paths; each path has some inherent delay requirement. These requirements derive from system performance goals, circuit functionality, system clock rates, interface timing constraints, and other considerations.

You can identify signal paths at any number of conceptual levels. A system-level path, for example, comprises a group of similar individual paths. All signals in the group have the same basic structure and requirements. For the system to operate properly, the signals must function within their requirements.

Once you identify a signal path and its requirements, timing analysis can determine if the path will meet its requirement. As with the identification process, you can perform timing analysis at any of several levels. You can scrutinize individual paths or analyze and take one or more paths from a system-level group to represent all of the paths in the group. Likewise, a number of analysis methods are available, depending on information availability and desired accuracy.

Maxima yield first-order estimates

You can make a good first-order timing estimate by adding the maximum delay values for each component in the path, which is called worst-case analysis. Most vendors provide data books that specify the maximum output propagation delays and input setup times for their devices. If the results of a worst-case analysis are within 20% of exceeding the path's timing requirement, that path is said to be critical and is usually subjected to more detailed analysis. If a path meets its requirements by 50% or more, it has a "safe margin," and no further analysis is necessary. Paths that fall somewhere between safe and critical may be treated either way but are usually reexamined along with the critical paths.

The worst-case-analysis method is simple to use, and often electrical CAE tools support it, allowing a majority of the signal paths in a design to be subjected to a first-order check. Passing this test does not guarantee, however, that a path will function properly. The estimate does not account for factors such as interchip wiring delays or driver loading effects. Generally, these effects are small, but for critical paths, they may be fatal. For this reason, designers use more rigorous worst-case methods that account for loading effects. Such methods first estimate the physical properties of the inter-

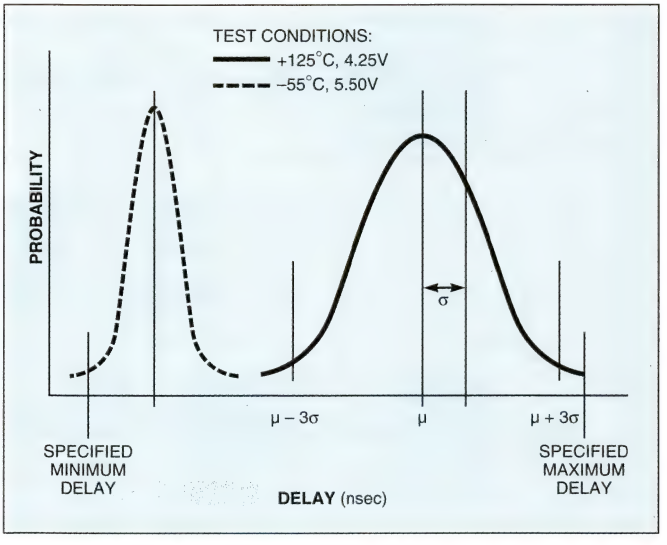

Fig 1—The delay distributions obtained at extreme operating conditions determine a part's minimum and maximum ratings. Using those distributions instead of maximum values lets you quantify your system's expected performance.

connections (length, capacitance, and inductance), then adjust the timing delays through each component or wiring segment in the path. You can perform the analysis manually using loading information from vendor data books or with the aid of a computer-based circuit-analysis tool.

Early in the design process, usually you do not have enough information to make an accurate estimate of the loading delays for each path. In such cases, the designer must make worst-case assumptions about the characteristics of a "typical node" (eg, all nodes have 35-pF load capacitance). Generally, designers also set a design margin that applies equally to a path in the design (eg, all paths must meet requirements by 10 nsec or more to allow for interchip delays).

For an example of a ROM-circuit analysis using the worst-case approach, see **box**, "A worst-case circuit analysis." In the example, the analysis predicts a delay of 122.2 nsec vs a requirement of 121.2 nsec. If, as in the example, the results of the worst-case analysis indicate that the circuit will not operate reliably over the specified range of operating conditions, conservative design rules dictate that you replace one or more of the components with a faster device, change the design, or relax performance goals.

This conservative approach can be prohibitive, especially for high-performance systems: System-level requirements usually restrict architectural changes, reducing performance goals is self-defeating, and in many cases, the fastest available parts have already been specified. When you can find faster parts, they are often expensive and available only in limited quantity, which limits the design's producibility.

Worst-case estimates conceal risk

At this point in the design process, most designers begin to rationalize, thinking it's not likely that all of the components in the path will perform at worst case, or they assume that vendors always pad the worst case specifications. Thus, a design team concludes that a marginal design will work fine in the real world. But how well the design will work is a question often left unanswered. The design team accepts the unknown risk and resolves to work it out on the prototype.

However, it is both possible and practical to quantify risks associated with a critical path. Statistical analysis offers

A worst-case circuit analysis

Fig A shows a typical system-level path in a microprocessor design. The path's starting point is the clock input of the memory-management unit (MMU). The signal path progresses from the clock to the MMU's A(0:16) and CS(0:3) outputs. From there, the signals travel to the address and control inputs of the ROM devices. The path asynchronously propagates through one of the ROMs and drives the inputs of a standard bus-interface device. The buffer interface in turn drives the microprocessor's data inputs (CPU).

Individual paths include many permutations of the same basic structure, which is a single control output propagating from the MMU clock input through the ROM and data buffers and into the CPU. In this case, 16 address bits and one chip-enable line traverse through three ROMs with eight data lines for (16+1)×3×8=408 individual paths. A single system-level path from MMU clock to CPU data input represents all of the individual paths.

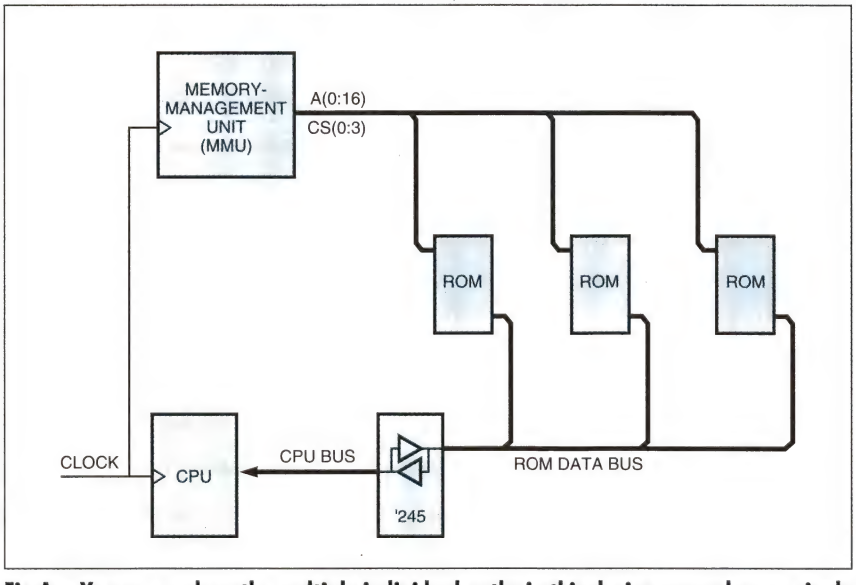

Fig A—You can analyze the multiple individual paths in this design example as a single system-level path.

Table 1 shows typical requirements for the microprocessor circuit in **Fig A**. To meet the 4-MIPS requirement at the 33-MHz clock rate, a typical instruction can require no more than 33/4=8 clock cycles. Instruction execution requires four clocks, so the ROMs must be accessed within four clock periods. Therefore, each of the 408 individual paths from the MMU clock input to the CPU data inputs must propagate in <4/33.0E+06=121.2 nsec.

Figure worst-case delays

In this example, the first-order worst-case analysis is straightforward. We have chosen to implement MMU functions using a field-programmable-gate-array (FPGA) device. Using the postlayout-timing-analysis tools the vendor provided, we find that the expected worst-case address delay is 12 nsec. The chip-select outputs are faster (8 nsec). According to the data book, the chip select to data delay of a ROM (50 nsec) is also faster than the address

detailed insight into path delays as well as a means for determining how well the design will work. The analysis methods use characterization data for each device—rather than maximum or minimum parameters—to derive a function that describes the probable delay for each device. Combining delay functions forms a joint probability distribution for the path's overall delay, which you then use to compute the probability that the path will either pass or fail its requirements. If all paths in the design receive a statistical analysis, you can estimate the design's expected manufacturing yield with respect to timing.

Few vendors actually publish characterization data for their products, yet this information is generally available through the vendor's technical-support staff. Most vendors collect product-characterization data to generate timing specifications for their parts and to provide metrics for monitoring their manufacturing processes. For military products, vendors must collect delay data to meet Mil-Std-883 requirements. If characterization data is not available from the vendor, however, you can collect it by measuring the delays through a large sample of devices (100 or more) over the design's desired range of temperatures and operating voltages. Note that such testing is usually expensive, though.

Using characterization data can be risky. Usually, characterization data is short-term data—for example, samples come from a single batch (lot) of devices produced over a short period of time. Short-term data does not account for the possibility that the manufacturer's processes may change over time or that multiple vendors (or multiple foundries owned by the same manufacturer) will produce the same end product with varying results. Also, characterization data can be wildly different from one manufacturer to another; and, currently, no standards exist for collecting this data.

Some vendors provide characterization data in statistical form: the mean (μ) and standard deviation (σ) or variance (σ^2) at a number of important temperature and voltage combinations over the specified operating conditions. Other vendors provide a table of measurements for a sample of devices under various environmental conditions. The data may represent either long- or short-term sampling, so the designer must take care to understand what type of information is

delay (90 nsec). Because the chip-select paths will always be faster than the address paths, we simplify the analysis by ignoring chip selects and concentrating on the worst-case address path.

The data buffer has a 7-nsec delay from input to output, and the CPU requires 5 nsec of setup time on data inputs. Therefore, the total worst-case delay is 12+90+7+5=114 nsec. Because this is within 20% of the requirement, (121.2–114)/ 121.2= 95%, consider the path critical. Thus, we need to examine wiring delays and loading effects.

In the case of our ROM circuit, the printed-wiring-board (PWB) vendor advertises typical capacitance of 4 pF/in. and inductance of 0.2 mH/in. of etch. An initial board layout suggests that each trace in the path has approximately 18 in. of etch. Computer models are not available for the CPU or FPGA pins, so you will have to estimate these by hand. The ROM manufacturer provided a Spice analysis of the ROM drivers and the buffer circuit based on our anticipated loading. We estimate the combined worst-case delay through this portion of the path to be 102.3 nsec, compared with 97 nsec using the first-order estimate.

For the MMU FPGA, the only loading information in the vendor's data book is a chart of delays vs capacitive loads. Inductive effects on these delays are small compared with capacitive loading, so, initially, we can ignore the inductive contribution and account only for capacitive effects. Calculate the load capacitance for a typical address line by adding the input capacitance of the three ROMs (12 pF×3=36 pF) and the anticipated capacitance of the signal trace (18 in.×4 pF/in.=72 pF) for a total of 108 pF.

The vendor-specified maximum delay of the output driver assumed a 50-pF load. The vendor's loading chart recommends adding to this maximum 0.05 nsec/pF over the rated load. The adjustment to the address delay through the MMU becomes 0.05× (108–50)=2.9 nsec. Therefore, total address delay through the MMU is 12+2.9=14.9 nsec. Because loading doesn't affect input setup delays, they remain at 5 nsec. Thus, total estimated delay for the ROM path is 14.9+ 102.3+5=122.2 nsec. The path fails to meet its requirement.

System example operating conditions

Average system throughput	>4 MIPS
System clock frequency	33 MHz
Processor software	ROM
Processor operation	(1) Opcodes prefetched during execution of previous instruction; (2) a typical instruction requires 4 internal clocks and makes 1 operand fetch; (3) memory-access cycles begin on the rising edge of a system clock. The MMU is programmed to extend the cycle by up to eight clock periods, and the process latches data inputs on the rising edge after the MMU signals that the cycle is ending.

available. From this information, the designer can derive a distribution function for a device delay at a number of important temperatures and operating voltages (**Fig 1**).

Calculating the delay distribution

The delay distribution function represents the probability that a randomly selected device will have a given delay under fixed operating conditions. In general, the distribution approximates a Gaussian, or normal, curve. The important statistical properties of the distribution are its mean (μ) and variance (σ^2). This information is directly available from statistical characterization data. For tabular data, the μ and σ^2 values must be calculated using **Eq 1** and **Eq 2** (**Ref 2**), where **X** is the series of delay measurements under the desired operating conditions, and **N** is the number of measurements.

$$\mu=\Sigma\mathbf{X}/\mathbf{N} \quad (1)$$

$$\sigma^2=\Sigma(\mathbf{X}-\mu)^2/\mathbf{N} \quad (2)$$

Note that temperature or voltage variations may affect both the mean and variance values in a nonlinear fashion. Designers, therefore, must recalculate μ and σ^2 for each desired set of operating conditions rather than simply scaling. Also, it is not generally valid to assume that a typical value in the vendor's data book represents the process mean or that the specified maximum values represent any specific variance from the process mean. Rather than making assumptions, designers should contact the vendor to obtain characterization data.

Most vendor-supplied characterization data is short-term data and does not account for the possibility that the vendor's manufacturing processes may change over time or that multiple factories or vendors may produce the product with varying results. Traditionally, vendors have accounted for such variations by specifying a guard band or design margin. Designers typically also include a design margin in their worst-case timing analysis by limiting the acceptable delay to some fixed value below the actual requirement. The trouble with these approaches is that they are arbitrary; it is virtually impossible to quantify risks associated with these methods.

Statistical analysis provides a more concise approach for handling short-term data; Motorola's Six Sigma approach offers two options: You either set the path goals such that the requirement is at least six standard deviations (6σ) greater than the mean delay for the path, or you account for possible process shifts by shifting the mean delay for each device by a factor of 1.5σ and then set the path goals such that no more than three defects are expected per million implementations (3 dpm) (**Ref 3**).

Some vendors track their processes and collect long-term characterization data. This data includes a large sample of devices from many manufacturing lots, and it accounts for normal process shifts by sampling the process over time. Depending on the vendor's record for controlling its processes, long-term data may provide more insight into the vendor's process shift than simply scaling short-term data. You can use long-term data directly, or, for a more conservative analysis, you can similarly scale it to short-term data.

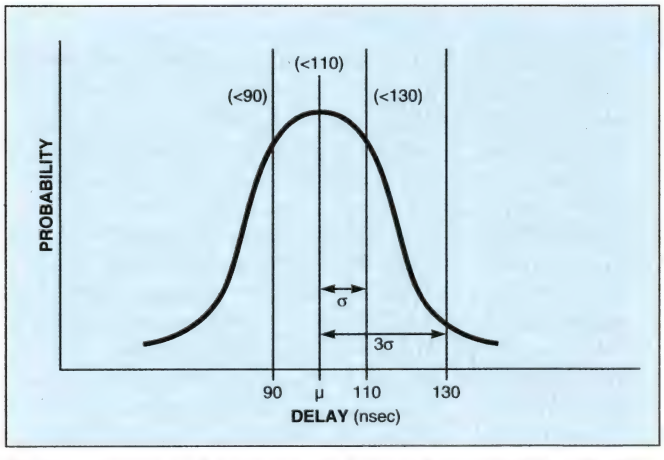

Fig 2—Products such as memories have a Gaussian delay distribution but are sorted into bins for sale by speed rating. Distributions within bins will not be Gaussian.

Statistics don't always apply

Some devices don't lend themselves to statistical modeling. Memory devices, for example, are produced in the same manner as most other electronic components but differ in how they are tested and sold. Most memory products are binned before shipment, meaning they are individually tested at the factory and sorted into groups that have similar performance characteristics. For example: A vendor manufactures ROMs that have a nominal access time of 100 nsec, and the variance for the process is 10 nsec. The vendor tests each part and sorts them into bins of <90 nsec, 90 to 110 nsec, and 110 to 130 nsec. Finally, the manufacturer marks each group of parts with an appropriate speed grade and sells the lots at different prices, based on market demand.

The delay distribution for each group is a part of the normal process distribution, but delays do not have normal distribution within a group (**Fig 2**). Because the distribution for a group of binned parts is not Gaussian, assume that the delay for that part will be equal to the vendor's specified maximum delay and that the variance of the group will be zero (ie, worst-case delay).

Field-programmable devices and ASICs offer another twist. Vendors cannot gather characterization information for a device that doesn't yet exist. However, the vendor can characterize the manufacturing process and provide timing analysis based on that characterization, estimating the delay distribution using a static timing analyzer. Most static timing analyzers can be set to determine "best/strong," "nominal," and "worst/weak" process points at minimum, nominal, and maximum temperature and supply voltage. By analyzing a path through the design at each of the process points—and holding the temperature at maximum and the supply voltage at minimum—designers can derive the worst-case delay distribution for the path.

As with other components, the delay distribution for an ASIC will be a Gaussian curve (unless the device is screened or speed-graded). The mean delay for the device is the result of the "nominal-process" timing analysis, and σ is given by

$$\sigma=(W-B)/2X, \quad (3)$$

where W is the result of the "worst-process" analysis, B is

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CIRCLE NO. 85

STATISTICAL TIMING ANALYSIS

the result of the "best-process" analysis, and X is the vendor's sigma metric. For most vendors, the sigma metric is 3 (ie, they use 3σ data for process corners). Verify the X value with the vendor.

Consider output loading

Another consideration when using characterization data is the effect of output loading. Vendors typically perform characterization with a 50-pF test load, which is true for ASIC-timing-analysis estimates as well. If the design loads are significantly more or less than the test load, an adjustment is necessary to account for loading. Like delays, loading adjustments can be modeled either as a worst-case value or as a statistical distribution based on variance in board layout and material properties. Currently, however, it is difficult to obtain statistical data for anticipated loading. To apply a worst-case loading adjustment to a statistical distribution, calculate the correction factor from the vendor's data book (same method as for worst-case analysis) and add this factor to the mean (μ) device delay.

Once you've modeled the delays statistically, you can derive a joint delay distribution for a critical path. Obtain the exact distribution by combining the distributions using the convolution integral: Convolve the distribution function of the first delay in the path with the second, and then convolve the result with the next delay, etc, until you combine all of the delay components. The result is the joint delay distribution for the path. Unfortunately, the mathematics for convolution are very complex.

Fortunately, the analysis can be simpler. For module-level paths that propagate through separate devices, the delay through each device usually can be considered to be independent of the other device delays (an exception would be a design composed of several identical devices that are all from the same manufacturing batch). In addition, each delay is randomly distributed within the delay distribution for that device. In this situation, the "root-sum-of-squares" (RSS) method allows use of the Central Limit Theorem in statistics to determine the joint distribution or overall delay characterization.

The Central Limit Theorem states that the sum of a set of such independent continuous random variables asymptotically approaches a normal distribution. This implies that the total path delay will have a Gaussian distribution with the mean equal to the sum of the individual path-delay means

$$\mu_J=\Sigma\mu \qquad (4)$$

and standard deviation related to the individual delay distributions by

$$\sigma_J=\sqrt{\Sigma\sigma^2}. \qquad (5)$$

Because the individual component distributions are considered normal, the error of this approximation is small—even for paths with only three or four components.

Sample statistical analysis

To reexamine the ROM path example (see **box**) using the RSS method, start by analyzing the memory-management unit (MMU) FPGA design. An initial analysis of all of the address- and chip-select paths indicates that the longest path is A(16). Because all of paths within the FPGA are highly correlated, you know that A(16) will always be the longest path, so you need only do detailed analysis on this one path. Rerunning the static timing analysis at 125°C, 4.5V, and all three process points yields 10.2, 11.1, and 12 nsec. Using **Eq 3**, σ=(12–10.2)/(2×3)=0.3 nsec. Because the 108-pF loading on the address lines is greater than the 50 pF assumed by the timing analyzer, you must adjust μ accordingly. The vendor's data book recommends adding 0.05 nsec/pF for loads greater than 50 pF, so

$$\mu=11.1+(0.05\times58)=14 \text{ nsec.}$$

According to the manufacturer, the CPU has a mean setup time of 4.5 nsec and variance of 0.17 nsec; the buffer device is specified to have mean propagation delay of 5.8 nsec and variance of 0.4 nsec. The ROM is a binned part, so use the maximum delay value (90 nsec) as the mean with zero variance. Add 4 nsec to the ROM delay to account for loading, making the mean delay 94 nsec with zero variance. Using **Eq 4** and **Eq 5**, the joint distribution for the path is a normal distribution with

$$\mu=14+94+5.8+4.5=118.3 \text{ nsec}$$
$$\sigma=\sqrt{(0.3^2)+(0^2)+(0.17^2)}=0.53 \text{ nsec.}$$

Once you know the joint distribution for a path, the probability (P_F) that the path delay will be greater than its requirement (ie, the path will fail) is given by the area under the distribution curve and to the right of the requirement (R) (**Fig 3**). You can calculate this area by evaluating

$$P=\int_R^\infty \left(\frac{1}{\sigma\sqrt{2\pi}}\right)e^{-(X-\mu)^2/(2\sigma^2)}dX \qquad (6)$$

However, because the distribution is considered to be a nor-

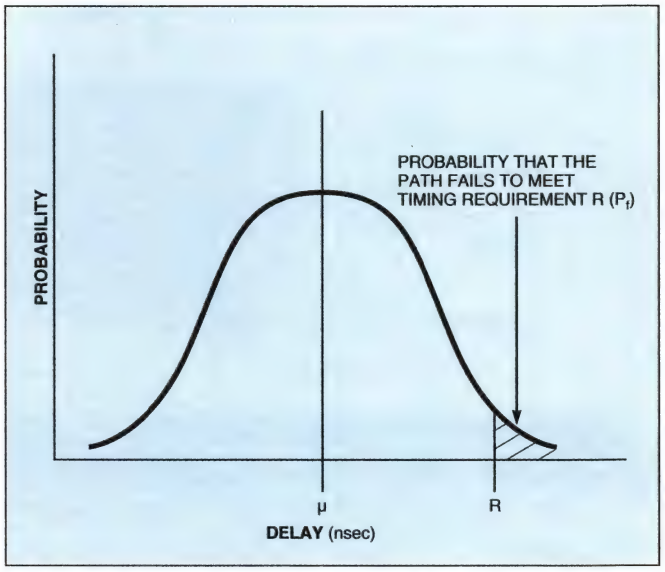

Fig 3—The probability that a path will fail to meet its timing requirement (R) is given by the area under the distribution curve to the right of R. This value may be calculated or determined from standard tables.

mal curve, a simpler method is to use a standard table of area under the normal curve (**Ref 3**).

Most standard tables of area under the normal curve contain either the area bounded by μ–z and μ+z; the tail area remaining below μ–z and above μ+z (bilateral tail area); the area left of μ+z (values of the normal distribution function); or the area remaining to the right of μ+z for positive values of z (unilateral tail area), where z is the sigma metric value given by

$$z=(R-\mu)/\sigma, \quad (7)$$

where R represents the value of the paths' required delay. By realizing that the total area under the normal curve is equal to 1, you can calculate the area remaining to the right of z using any table of area under the normal curve.

For the ROM path, z=(121.2–118.3)/0.53=5.47. Because short-term data was used to calculate μ and σ for the path, the initial Six Sigma goal is z>6. Although the goal isn't met, you still may be willing to accept the risks for this high-performance design. To better quantify the risk, you can approximate the long-term distribution for the path by adding 1.5σ to μ. Reevaluation of **Eq 7** yields

$$z=(121.2-(118.3+0.795))/0.53=3.97.$$

A standard table of area under the normal curve lists the area remaining to the right of 3.97σ as 3.606E–05 (**Ref 3**). The probability that a given ROM address path will fail is 1/3.606E–05 or 1 in 27,732 or 36 dpm. Again, you didn't meet the Six Sigma goal of ≤3 dpm. However, you've quantified the risk. Depending on the expected manufacturing volume and cost of producing a faulty unit, the project may accept the risk for this high-performance system.

Another tool that can help the designer quantify risk is the system-level yield calculation. If you perform an RSS analysis for several independent paths in the design, compute the overall probability that one of the paths will fail (P_{SF}) using

$$P_{SF}=1-\{(1-P_F(1))\times(1-P_F(2))\times(1-P_F(3))\ldots\times(1-P_F(N))\}. \quad (8)$$

For this type of system-level calculation, it's important to realize that paths are not always independent. There is generally a high correlation between individual delay paths through a single IC (the variances of address to data delays through a ROM will be close to identical). When parallel paths all run through the same devices, if the slowest path passes, it is likely that all of the others will pass. Therefore, the probability that a system-level path will fail is approximately the probability that the slowest path will fail.

When using statistical methods, take care to understand the assumptions of statistical analysis and to know when to apply these methods. In the example, we calculated the probability that the slowest ROM path will fail. Ignoring the faster enable paths, the probability that the system-level ROM path will fail is simply the probability that any one of the 384 permutations of the address paths will fail. If you apply **Eq 8** directly, the probability is $1-(1-0.606E-05)^{384}=0.013$. You'd expect one in 72 of the boards to fail manufacturing test due to a ROM failure.

This result is incorrect. All of the paths that pass through a single ROM have a strong correlation, so **Eq 8** does not apply. The probability that any of these paths will fail is approximately the probability that the slowest ROM address path will fail, or 3.606E-05. Because the system has three ROMs, the probability that the ROM function will fail is $1-(1-3.606E-05)^3=1.082E-04$. You should expect only one in 9244 boards to fail as a result of a ROM-address-path failure.

Use **Eq 8** to combine probabilities for separate paths such as the address and chip-select paths. If the probability that a ROM chip-select path will fail is 1.23E-06, the probability the ROM function will fail is $1-\{(1-1.23E-06)^3\times(1-3.606E-05)^3\}=1.12$ E-04, or one in 8937 boards.

Finally, the probability that all of the paths on the board will pass, called the system-level yield, is given by

$$Y=1-P_{SF}. \quad (9)$$

For the ROM function, the yield with respect to timing is 1–1.12E-04 or 0.999888, meaning 99.98% of the boards will operate properly. Of course this doesn't account for other potentially critical paths in the design. Further analysis will establish a good estimate of the system-level yield for the entire design.

When analyzing the entire design, use both statistical and worst-case methods. Worst-case methods provide a fast, simple approach to help identify critical timing concerns. While conservative, they tend to ensure high reliability of the final product. Statistical methods can help quantify risks allowing you to make informed decisions to balance performance, cost, and manufacturability goals. Together, worst-case and statistical methods combine as a powerful design tool. EDN

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Author's biography

James J Vorgert is an electrical design engineer with the Corporate Venture Products Group of Texas Instruments, where he currently designs both digital and analog circuit boards. For four years, he worked as a CAE-design methodology specialist with TI's Defense Systems and Electronics Group. He has a BSEE from the University of Minnesota and enjoys photography, woodworking, and backpacking in his spare time.

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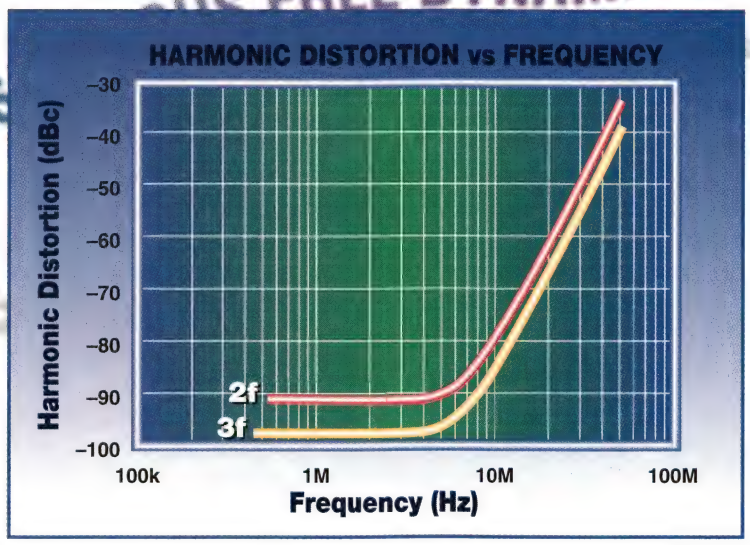

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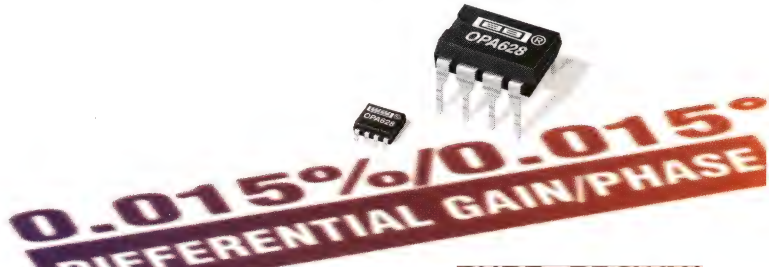

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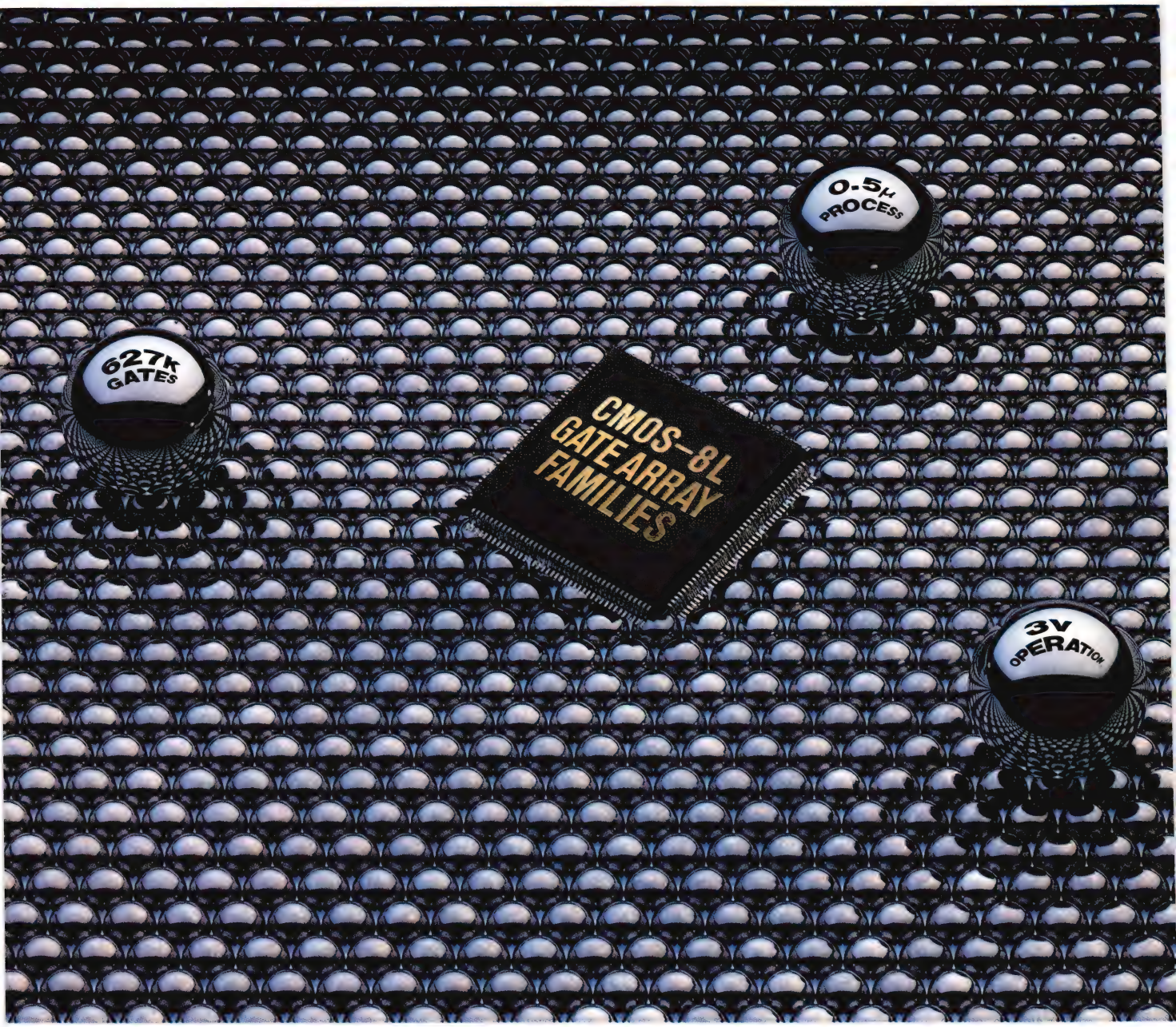

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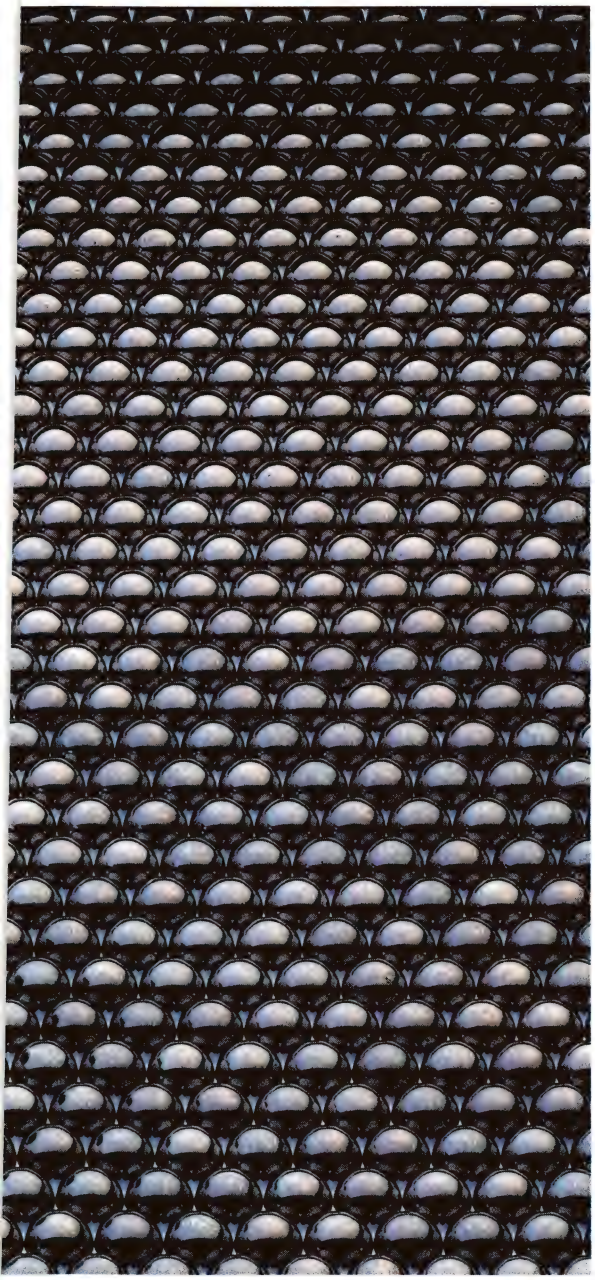

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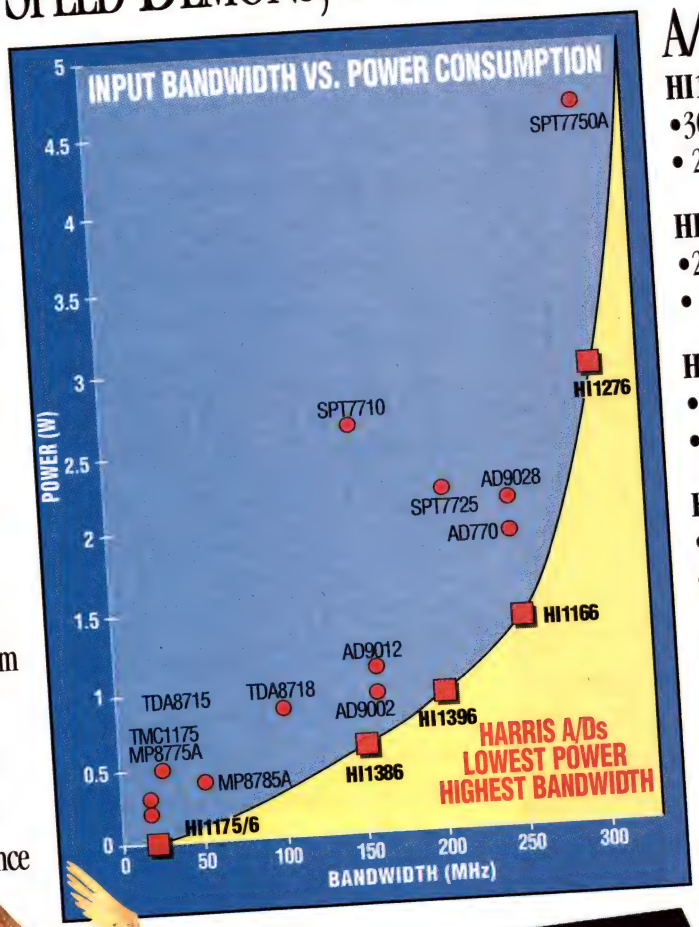

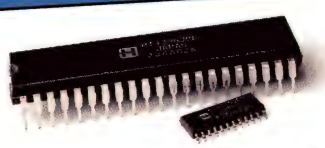

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CIRCLE NO. 82

Minimize time delays and reduce circuit density by retiming a design

Jaap Sondervan, Philips Electronic Design and Tools

Timing for initial sequential circuit designs generally is not optimal. By following some retiming procedures, you can add or delete sequential blocks to optimize circuit timing requirements and minimize circuitry.

Retiming is a basic technique for modifying digital circuits' clocking behavior without changing the circuits' functionality. Because the sequential part of many designs involves flip-flops, you can retime a circuit by adding, deleting, or shifting flip-flops in the basic circuit until you achieve desired timing results. The goal of retiming a circuit is to achieve a desired clock rate and simultaneously reduce the circuit density by using a minimum number of flip-flops. In addition, retiming a circuit can create a pipeline architecture by adding or deleting flip-flop stages.

Retiming should change only the timing relationship of signals by advancing or postponing exactly one or more clock cycles. A basic rule for retiming a circuit is that you can freely insert flip-flops into a network or shift a flip-flop through a node within the network (provided timing relationships between branches don't change). If you encounter a fork in the network, you may have to insert more than one flip-flop after the node to maintain the same timing relationship. If multiple network paths join at one node, you can reduce the number of flip-flops preceding the node to one flip-flop after the node.

Fig 1 illustrates this idea: (**a**) shows a simple node without a pipeline state; (**b**) inserts a flip-flop before the node, which creates a pipeline architecture. In this architecture, the flip-flop drives both nodes. However, you can maintain the same timing relationships by shifting the flip-flop through the node and adding a flip-flop in each branch after the node (**c**). **Fig 2** illustrates how you can shift flip-flops (or registers) through a node even when the node is connected by combinatorial logic. A vertical bar depicts the flip-flops (or registers) in **Fig 2** and will be a convention throughout the rest of this article.

As a practical application for retiming a circuit, consider the FIR filter in **Fig 3**. The output of the filter is given as

$$O=I+I_{-1}+I_{-2}.$$

In the basic circuit of **Fig 3**(**a**), two registers delay the input signal (I) to develop the I_{-1} and I_{-2} signals. The time delays of the two adder blocks are in the critical path of the circuit and create a limit to the maximum-output clock frequency attainable. Using the basic rules for retiming lets you shift the registers through the nodes in the circuit, provided you maintain the equivalent timing relationships between branches.

In **Fig 3**(**b**), the rule allows registers FF1A and FF1B to replace register FF1. Register FF2 shifts to a new position

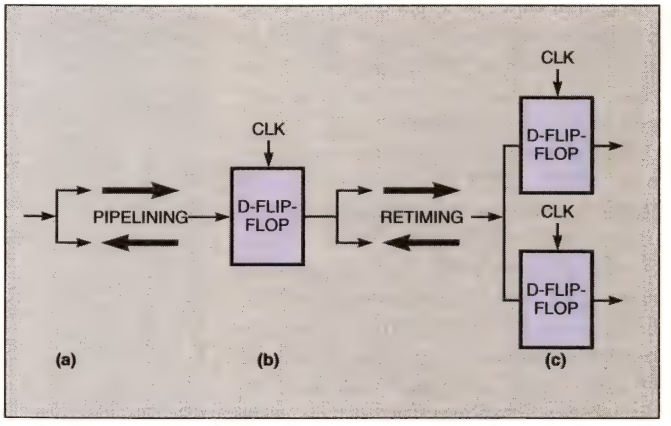

Fig 1—Inserting a flip-flop into the path of a circuit creates a pipeline stage. To retime the pipelined circuit, shift the flip-flop through the node to add two flip-flops to the two succeeding branches.

BBS

The software listings in this article are available on EDN's computer bulletin-board system (BBS). Phone (617) 558-4241 with modem settings 300/1200/2400 8,N,1. Access */freeware* SIG and specify *(r)ead* option followed by *(k)eyword* search for "MS #687."

RETIMING SEQUENTIAL CIRCUITS

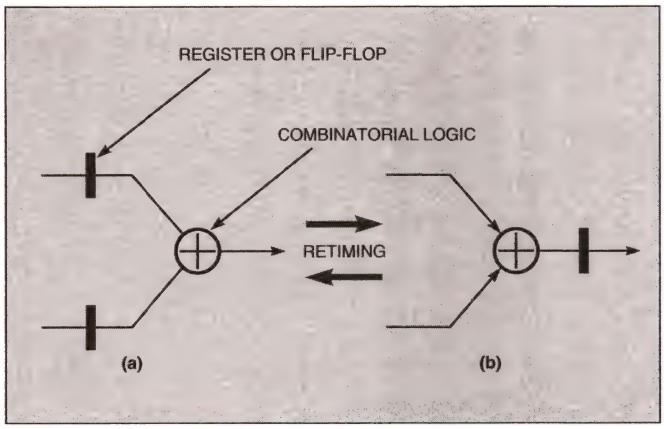

Fig 2—You can shift flip-flops through a node to retime a circuit even though the node consists of combinatorial logic.

in the same branch. Essentially, the functional operation of the circuit has not changed. The next step in the retiming procedure is to consolidate registers FF1A and FF1B into one register that resides between the adders (**c**). The final circuit (**d**) now has only the time delay of one adder in the critical path. The final circuit will operate at twice the frequency of the original circuit. Note that the circuit-performance increase occurs without any increase in circuit density.

Another example of retiming is the pipeline architecture of **Fig 4**. In **Fig 4(b)**, an additional pipeline stage (FF4 and FF3) is inserted in the positions indicated relative to the original circuit (**a**). The result of the register addition means the time delay due to combinatorial logic halves, but the output is available one clock cycle later. A timing diagram would show that the time between clock periods for the original circuit could exceed an entire clock period due to the time delays of two combinatorial blocks. Although the output of the final circuit exceeds the clock period by one clock cycle due to the added pipeline registers, the delay between successive clock cycles is shorter than a clock period. This results because the time delay is only one combinatorial block.

Retiming techniques are not new, but today, CAD procedures handle these techniques automatically instead of manually. CAD procedures usually consist of two techniques. A postoptimizer technique relocates existing flip-flops; a design-tool technique allocates pipeline stages. Using the postoptimizer technique, you insert flip-flops (or registers) by schematic entry—or by high-level description language if using synthesis. Often the positioning of the flip-flops is not optimal.

The pipelined architecture in **Fig 5(a)** could have been created by synthesis or schematic entry. The example has a maximum time delay of four logic gates between the four flip-flops in the branches and the flip-flop in the output path. After design entry, you can postoptimize this design using retiming. The modified design must exhibit the same functionality as the original circuit; therefore, the number of pipeline stages between the inputs and the output must not change. This restriction is called "keeping the latency."

You have a number of ways to postoptimize this design. **Fig 5(b)** demonstrates one way, which minimizes chip density but maintains a maximum time delay of six logic gates. Achieve the optimized design by shifting the flip-flops in the branches through the combinatorial node to the output path. The design also achieves a power-dissipation reduction, from five to two flip-flops. **Fig 5(c)** shows another postoptimized design of the original circuit. By moving the four flip-flops in the input branches through the secondary branch nodes, you achieve a maximum time delay of three logic stages. The number of flip-flops decreases from five to three.

Using CAD procedures, a top-down design comprises the following steps: First, make a behavioral high-level description of the circuit. When the behavior is correct, transform the description into a Register Transfer Level (RTL) description. Manually add logical structure to the RTL description to perform gate-level synthesis; you need the additional structure because state-of-the-art gate-level-synthesis tools cannot synthesize sequential operations (except for the special case of state machines, where flip-flops are implicit in the description). Adding structure man-

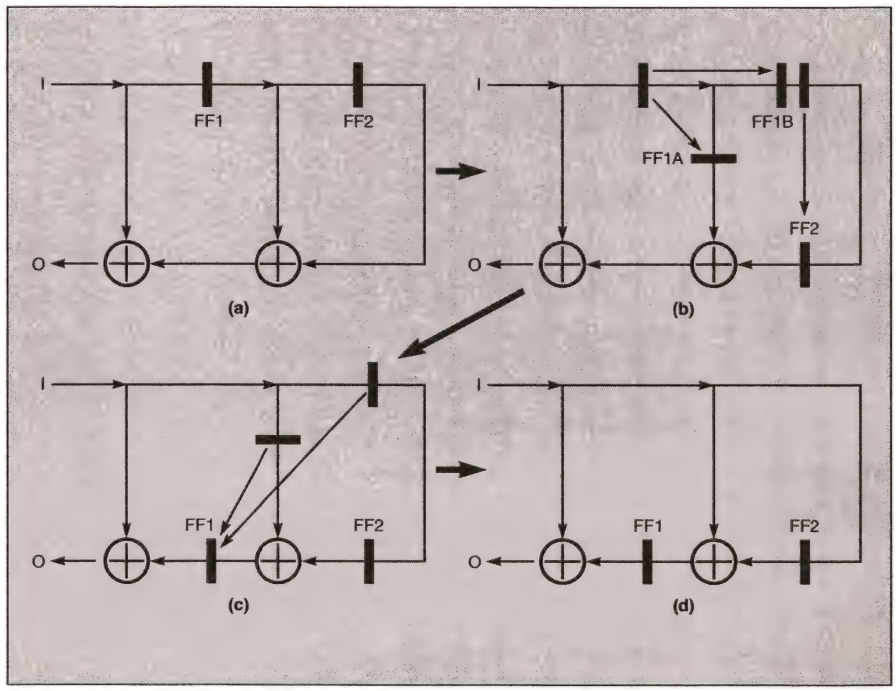

Fig 3—In this example of an FIR filter, the original circuit (a) suffers the time delay of two adders in the output path. After the circuit is retimed (d), the time delay is reduced to one adder.

APRIL 19,1993 • PC WEEK

from pag

"...Standard alkaline batteries are available anywhere, while NiCad and NiMH batteries can be purchased – in hundreds of variations – only through computer dealers or the manufacturers of portable PCs. Industry heavyweight Duracell Inc. seeks to lessen that inconvenience."

"...Cellular phone manufacturers can benefit from economies of scale provided by mass-produced battery packs and can then leverage the fact that replacement battery packs are available at mass retail wherever their devices are sold."

36 ***Cellular Business*** April 1993

"...Standard battery packs would relieve portable PC manufacturers from having to custom-design their own rechargeable batteries...That should yield savings in both production time and costs."

January 12, 1993 PC MAGAZINE 3

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CIRCLE NO. 79

RETIMING SEQUENTIAL CIRCUITS

ually is tedious because it usually takes one or more iterations to meet design constraints. **Fig 6** depicts the top-down procedure.

Refer to **Listing 1** (see *EDN* BBS) for an example of the behavioral VHDL (VHSIC hardware-description language) code for a 32-bit comparator. Typical synthesis for this design's VHDL code using the LSI Logic LCA100k library results in 426 gates having an overall time delay of 21 nsec. Because the specification requires a maximum time delay of 15 nsec, the design has to be pipelined. To pipeline the design, the RTL description must be changed manually. **Listing 2** (see *EDN* BBS) shows the resulting RTL-VHDL source code. The synthesized design results in a time delay of 11 nsec using two pipeline stages consisting of 20 flip-flops.

You can retime the design using Optima, a retiming tool from Philips Electronic Design and Tools, to create a pipeline that has exactly 15-nsec time delay. Using Optima, you can specify the time-delay constraint to be exactly 15 nsec. Optima produces a design that has one pipeline stage using eight flip-flops, which is fewer than the synthesized manual design. You could also find the optimized design that uses only one pipeline stage to achieve the shortest time delay. This design results in a time delay of 12 nsec using 17 flip-flops. EDN

Author's biography

Jaap B Sondervan is a marketing manager for Philips Electronic Design and Tools in The Netherlands. Sondervan specializes in CAD-product marketing and public relations and has been with Philips for nine years. His main interests are in synthesis and test for ASICs. Sondervan has an MSC in Electronic Engineering.

Article Interest Quotient (Circle One)
High 595 Medium 596 Low 597

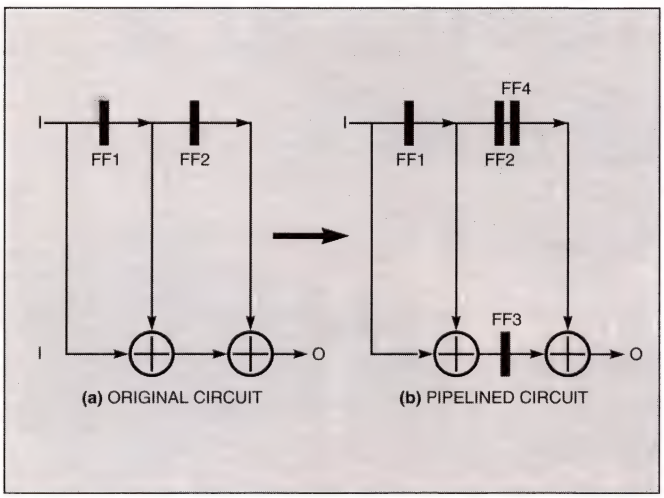

Fig 4—The original pipelined circuit (a) suffers the time delay of two adders in the output path. Retiming the circuit (b) creates another pipeline stage but reduces the time delay to one adder in the output path.

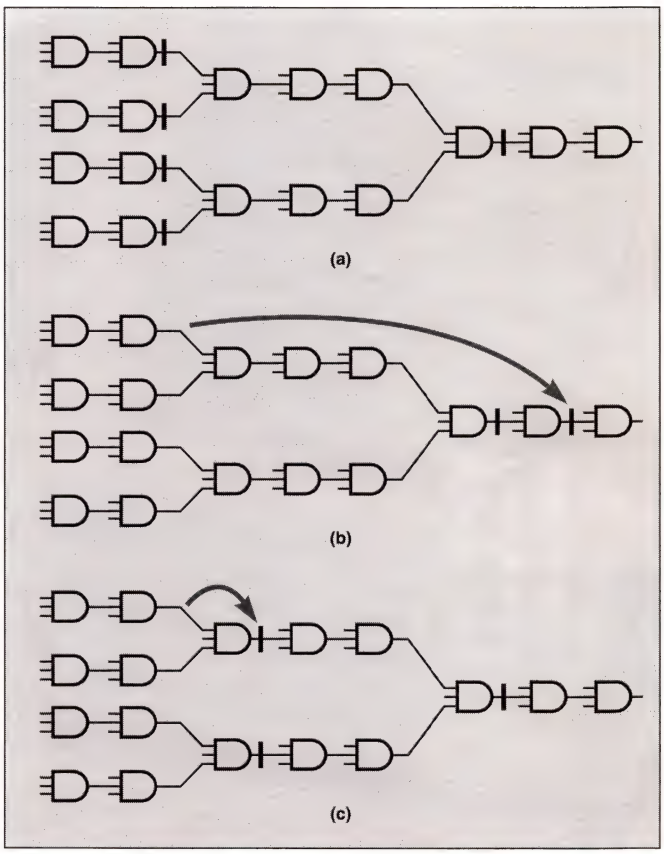

Fig 5—You can retime this synthesized circuit (a), which has time delays for four logic gates, in a variety of ways. Two examples appear in (b) and (c).

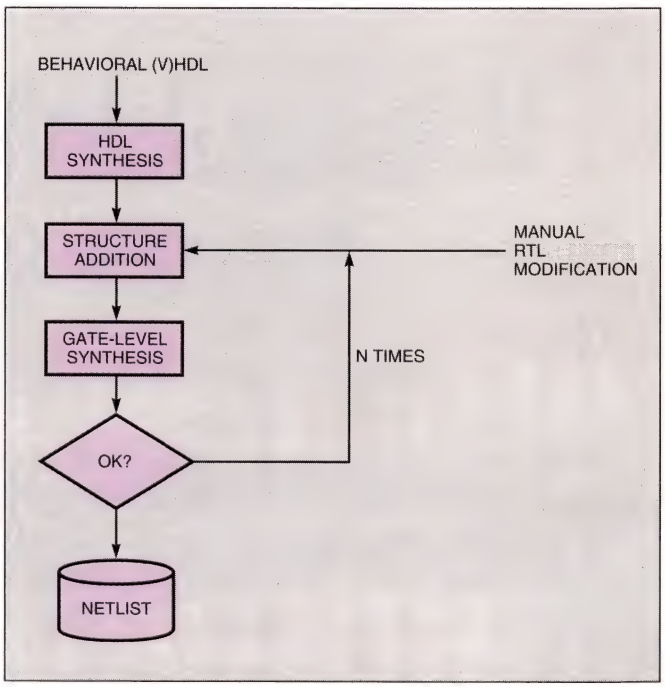

Fig 6—A top-down procedure for manually designing a pipelined architecture requires many repetitive modifications.

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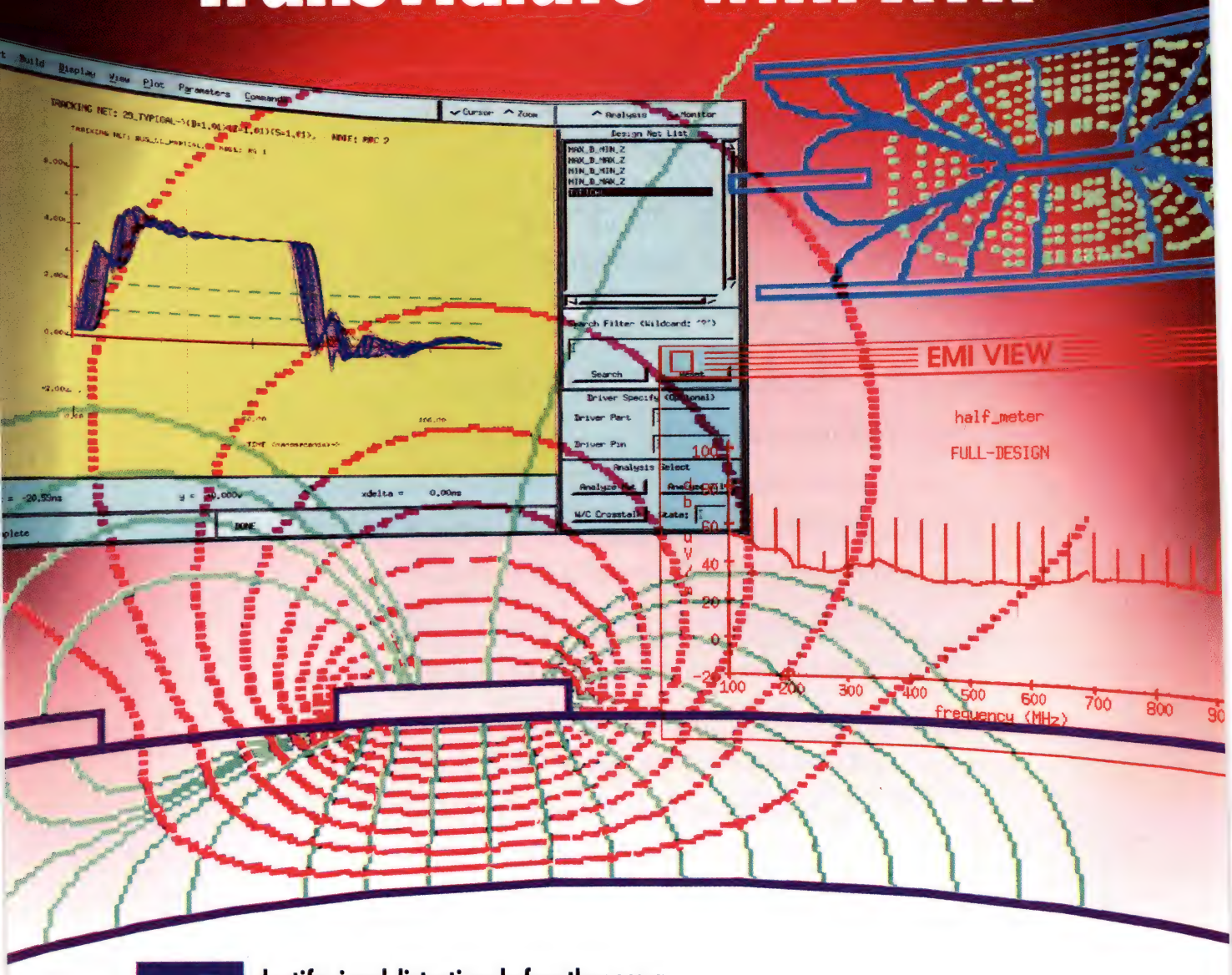

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CIRCLE NO. 102

Kit evaluates low-power applications

Designing a low-power system is not just a matter of connecting low-power components. To lower power, you make tradeoffs between running full speed and reducing performance. You also must ensure that your software takes advantage of the hardware's power-saving capabilities and you should take advantage of a variety of power-saving features on modern μCs (microcontrollers).

But it isn't easy to decide which features provide the lowest power: How much will lowering the clock speed, placing the μC in standby mode, lowering the voltage, or changing your code affect the battery life of your design?

This evaluation kit allows you to learn more about low-power system design; you can play games with clock speeds, supply voltage, and code.

The M68EBLP11KIT evaluation kit helps find answers to these questions. Based on the Motorola 68HC11E9 μC, the kit consists of an evaluation board, development code, a low-power-design manual, technical documentation, extra crystals—and yes, even batteries.

The evaluation board contains the μC, a 14-character, 2-line LCD, an RS-232C interface, low-power LCD driver chips, a wire-wrap area, and a battery holder. The 68HC11E9 μC has 512 bytes of RAM and EEPROM, 38 I/O lines, and an 8-channel, 8-bit ADC.

A typical application runs from two weeks to a month using batteries. If you often use standby mode, battery life can last up to two months; full out, without any standby, reduces battery life to 30 to 40 hours.

You don't have to use three AA batteries. You can also power the board with a regulated power supply (2.7 to 5.5V dc) or unregulated power (7.5 to 15V dc).

By changing clock frequency, you can experiment with clock-speed tradeoffs. You can find out if your application would benefit from running at a higher clock frequency with longer standby times or a slower clock frequency with less time to sit in standby mode.

Preprogrammed into the 12-kbyte ROM on the μC is a monitor program called BUFFALO, which includes a debugger and a 1-line assembler/disassembler. You can also download assembled code developed on your computer.

Once you figure out your application, enter it in Motorola's Portable Power Design Contest, which offers a chance to win $511 and a chance to have your entry published by Motorola.

—David Shear

Motorola, Austin, TX. (512) 891-3465.
Circle No. 332

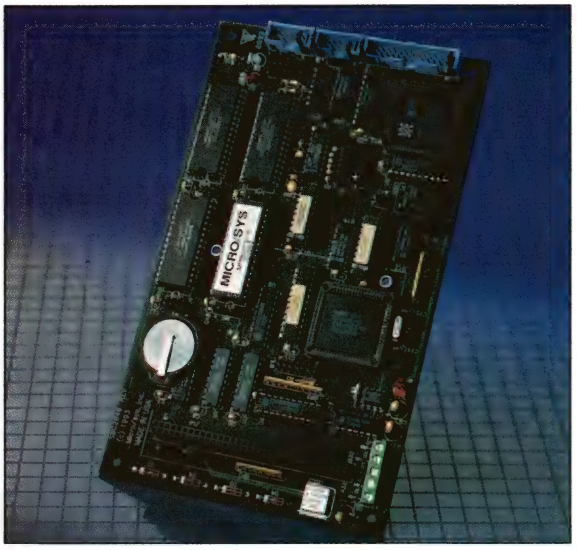
Single-board PC includes onboard development firmware

Often, developing low-end PC-based embedded systems requires that you load various tools into the target to debug your code. In these applications, a keyboard and video display may not exist on the target. Borland's TDREMOTE, a target-resident utility, allows you to use the company's Turbo Debugger on the target system.

The SBC2040 includes firmware that can support Borland's Turbo Debugger. You just connect a cable between the PC and the SBC2040. When you've debugged the program, the unmodified .exe file is burned into EPROM and plugged into the SBC2040. A flash EEPROM package is available for field upgrades.

The single-board computer suits diskless applications and includes two serial ports, a parallel port, and a watchdog timer. Onboard memory handles four 32-pin memory ICs, for a total of up to 4 Mbytes of memory. A PC/104 interface and a 6-channel 12-bit A/D converter are also included. $275; $75 for the A/D option.**—David Shear**

Micro/Sys, Glendale, CA. (818) 244-4600.
Circle No. 333



To get started debugging your code, all you do is connect a serial cable between this PC-based single-board computer and your PC.

DSP development board includes integrated SVGA graphics system

The DSP Lab One signal-processing board combines a DSP development system with an SVGA graphics system on one ISA board. The board lets you acquire data, process it, and then display the results on a monitor without impacting the operation of the PC it's plugged into.

By separating the DSP functions (including displaying data) from the PC, you have complete access to the PC for other operations while developing algorithms. You can also use the PC as the human interface and modify the operation of the DSP system while the DSP system runs.

The board contains four Texas Instruments TMS320C51 DSPs, 16-bit A/D and D/A converters (166-kHz maximum sample rate), a TMS34010-based SVGA graphics controller, and 2.5 Mbytes of onboard memory. The DSPs communicate with the host and each other via global memory and high-speed serial buses.

Tutorials, sample displays, sample applications, a monitor/loader, and high-level graphics functions are also included. The SAL-DL1/28 runs at 28 MHz and costs $3995; the 20-MHz SAL-DL1/20 costs $3495.—**David Shear**

Standing Applications Laboratory, Kirkland, WA. (206) 453-7855.

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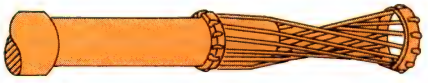

Pin partially inserted into sleeve.

Pin completely inserted into sleeve.

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CIRCLE NO. 83

Motorola 8-bit μCs head for 1.8, 3V operation

A tidal wave of low-power applications is crashing against engineering shores. Burgeoning applications include remote controls, pagers, cellular and portable phones, video games, cameras, handheld audio and video, notebook computers, and handheld digital assistants. Low-power 8-bit μCs supply the smarts to control these products. Motorola's 8-bit controllers, the popular 68HC05 and 68HC08 families, are available in low-power versions.

Motorola's low-end 68HC05 now comes in low-power 1.8V versions. Initially, seven members of the 8-bit 68HC05 family can operate at 1.8V, running with a 500-MHz clock. These μCs cut power significantly for power-limited applications over 5V—or even 3V parts. (Power is a function of the square of the voltage.) The 68HC05 has handled 3 and 5V operation since its introduction in 1984. Bus clock rates for 5V

Motorola low-voltage 68HC11 8-bit μCs

Part	ROM (kbytes)	RAM (bytes)	EEPROM (bytes)	I/O pins	A/D (8 bit)	Bus speed (MHz)	Package type
68HC11A8 series	8	256	512	38	Yes	0 to 2	52-pin PLCC 48-pin DIP 64-pin QFP
68HC11D3 series	4	192	N/A	32	Yes	0 to 2	40-pin DIP 44-pin QFP 52-pin TQFP
68HC11E9 series	12	512	512	38	Yes	0 to 2	52-pin PLCC 52-pin TQFP 64-pin QFP
68HC11F1	N/A	1	512	30	Yes	0 to 3	68-pin PLCC 80-pin TQFP
68HC11K4 series	24	768	640	62	Yes	0 to 3	84-pin PLCC 80-pin QFP
68HC11KA4 series	24	768	640	51	Yes	0 to 3	68-pin PLCC
68HC11L6 series	16	512	512	46	Yes	0 to 2	68-pin PLCC 64-pin QFP

MICROPROCESSORS

parts go to 2 MHz (1 MHz for 3V parts).

Motorola has also reinforced the low-power ranks of its mainline 68HC11 with new parts. These include a ROM-less part (the 678HCF1) and three ROM/EPROM parts, with up to 24 kbytes of on-chip ROM. All these chips have an 8-bit A/D converter and 512 or 640 bytes of EEPROM to hold application-specific constants and codes. All the 3V 68HC11 parts run at the same bus clock rates as the higher voltage, 5V chips.

Motorola 1.8V 68HC05 8-bit μCs

Part	ROM (kbytes)	RAM (bytes)	Timer (bits)	I/O pins	Bus speed (kHz)	Package
68HC05C4	8	176	16	28	0 to 500	40-pin DIP 44-pin PLCC/QFP 42-pin SDIP
68HC05C8	4	176	16	28	0 to 500	40-pin DIP 44-pin PLCC/QFP 42-pin SDIP
68HC05C12	12	176	16	28	0 to 500	40-pin DIP 44-pin PLCC/QFP 42-pin SDIP
68HC05J1A	1	64	Multi	14	0 to 500	20-pin DIP 20-pin SOIC
68HC05K0	0.5	128	Multi	10	0 to 500	16-pin DIP 16-pin SOIC
68HC05P1	2	768	16	20	0 to 500	28-pin DIP 28-pin DIP 28-pin SOIC
68HC05P4	4	768	16	20	0 to 500	28-pin DIP 28-pin SOIC

For the 68HC11 low-voltage parts, Motorola supplies a battery-powered development board and kit, with a tutorial and development software. The 3V 68HC11 family: D3, $4.34; A8, $7.52; E9, $8.57; L6, $10.86. For the lower-level 1.8V 68HC05 line, prices start at $1.07 for a K0; 3 to 5V K0 parts cost $0.98 (50,000).—**Ray Weiss**

Motorola Inc, Austin, TX. (512) 891-2000. **Circle No. 579**

Generator produces 100V or 2A pulses with 100-psec timing resolution. The 8114A generator ($9600) produces pulses to 15 MHz. It provides a variable duty cycle and 7-nsec transitions. Amplitude resolution is 10 mV, and amplitude error is <1%. A $1700 variable-baseline option lets you offset the output up to ±25V. **Hewlett-Packard Co**, Santa Clara, CA. (800) 452-4844. **Circle No. 346**

Monitor displays NTSC, PAL, and SECAM waveforms. The Model 5222 monitor handles composite and component waveforms simultaneously. The monitor has two groups of four inputs. It derives sync from two inputs in each group plus an external reference. The unit produces overlay, parade, and picture displays. A white phosphor is optional. Cursors control on-screen signal-parameter readouts. Menus control the instrument setup; the unit stores and recalls 10 of these setups. $3665. **Leader Instruments Corp**, Hauppauge, NY. (516) 231-6900. **Circle No. 347**

IEEE-488 interface runs under MS-Windows V3.1. The 82341A occupies one ISA- or EISA-bus slot. The software that accompanies the board enables you to write C or C++ programs that import data into Windows applications from any instrument that has an IEEE-488.2 interface. $495. Version for Windows NT, $845. Upgrade from Windows to Windows NT version, $350. **Hewlett-Packard Co**, Santa Clara, CA. (800) 452-4844. **Circle No. 348**

C-size VXIbus digital I/O module handles 96 channels. The 1277-5A includes 12 8-channel groups. You can program any group to act as inputs or outputs. Each line can source or sink 100 mA. Each output has separate thresholds for logic 1 and logic 0. Using external power supplies, you can set these thresholds from +50 to –50V. $11,540; delivery eight to 10 weeks, ARO. **Racal Instruments**, Irvine, CA. (800) 722-3262. **Circle No. 349**

Data-acquisition packages' universal driver supports ISA-bus boards and IEEE-488 and RS-232C instruments. The Universal data-acquisition driver that now comes with Labtech Notebook and Labtech Control provides the same flexibility as the universal printer drivers that have been a staple of PC word processors for many years. With the Windows versions of the data-acquisition and -control packages, you can intermix instruments from multiple vendors. With the DOS versions, memory limitations restrict you to hardware from one vendor at a time. The packages' prices start at $995. **Laboratory Technologies Corp**, Wilmington, MA. (508) 657-5400. **Circle No. 350**

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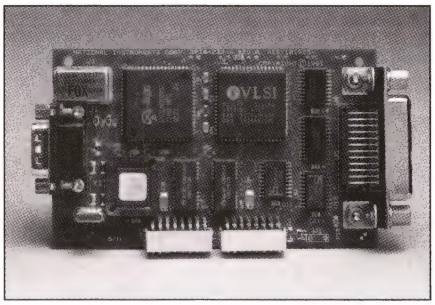

Cards that mount within instruments convert between IEEE-488 and RS-232C. The GPIB-232CV-A (OEM) lets you connect an instrument that has an RS-232C port to the IEEE-488 bus. The GPIB-232CT-A (OEM) lets a controller or terminal that has an RS-232C port act as a full-functioned IEEE-488.2 controller. This unit implements normal and extended talker and listener modes, serial and parallel polling, service requests, passing and receiving of control functions, and remote programming. Each board costs $495 (one). **National Instruments Corp**, Austin, TX. (512) 794-0100. **Circle No. 351**

Benchtop power supply provides up to 35V and 1.7A. The E3616A power supply has 10-turn potentiometers that control output voltage and current. A pair of digital meters monitors both quantities simultaneously. Line and load regulation are each 0.01%. Remote sensing compensates for I-R drops in external wiring. Output noise is <200 μV rms. $500. **Hewlett-Packard Co**, Santa Clara, CA. (800) 452-4844. **Circle No. 352**

PC-based fax protocol analyzer displays T.30 handshakes as well as T.4 image data. The GD-Fax 14.4 passively monitors a phone line and captures all data traveling in both directions between a pair of fax machines or fax boards. It then displays the data and a detailed analysis of timing information, deviations from CCITT standards, and data or format errors. $4495, including a year of software updates. **Gray Associates**, Truckee, CA. (916) 582-8623. **Circle No. 353**

IEEE-488-programmable resistance calibrators limit error to 0.002% from 100Ω to 1.9 MΩ. You can operate the 6201 and 6202 calibrators from their front panels or via the IEEE-488 bus. The 6201 ($2600) provides decade values from 1Ω to 10 MΩ. The 6202 ($3500) provides all of these values as well as values 1.9× as great. (In other words, the 6202 provides twice as many values as the 6201, the highest being 19 MΩ.) The units allow you to make 2- or 4-wire connections. **Electronic Development Corp**, Boston, MA. (617) 268-9696. **Circle No. 354**

Programmable linear power supplies produce single and dual outputs to 240W. The single-output PM 2831 ($2095) and the dual-output PM 2832 ($3595) power supplies operate as voltage or current sources with automatic crossover. Each output provides up to 8V dc at up to 15A. You can program the overvoltage and overcurrent limits separately from the output values. Output voltage resolution is 2 mV; output current resolution is 0.75 mA. The units operate in two quadrants; that is, their outputs can source or sink current. Programming is via IEEE-488.2; the command set conforms to the SCPI syntax. The units store 99 output settings and can automatically step through them. **Fluke Corp**, Everett, WA. (800) 443-5853. **Circle No. 355**

VXIbus interface software runs under LynxOS real-time OS. The NI-VXI software for LynxOS includes a resource manager, a VXI resource editor, a library of routines for VXI programming, and an interactive control program for debugging the VXIbus. The software can configure and control VXI systems that comprise single or multiple mainframes. $995. **National Instruments Corp**, Austin, TX. (512) 794-0100. **Circle No. 356**

ISA-bus card houses 12-MHz direct digital synthesizer. The DDS3, which resolves 2 Hz, plugs into an 8-bit ISA bus. It generates sine

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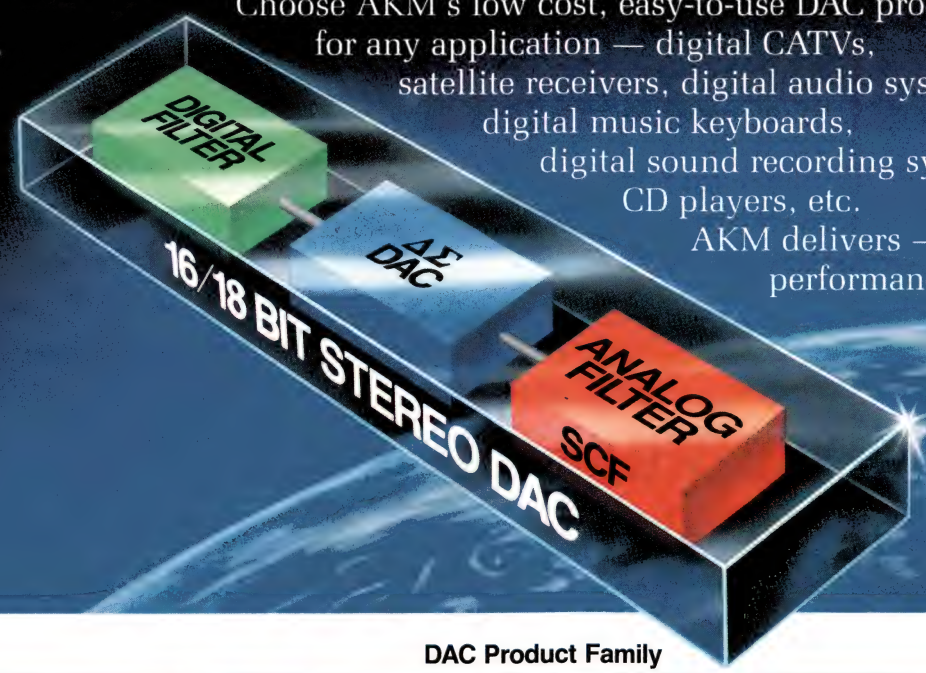

DAC Product Family

Device	# of bits	DR	S/N	THD + N	Special Features	Voltage
AK4316	16	90dB	90dB	0.01%	• High tolerance to clock jitter	+5V
AK4318	18	97dB	97dB	0.0025%	• High tolerance to clock jitter • De-emphasis control circuit • Soft mute function	+5V
AK4313	18	93dB	93dB	0.004%	• High tolerance to clock jitter • De-emphasis control circuit • Soft mute function • Low voltage	2.7~4.0V

AKM

Asahi Kasei Microsystems Co.,Ltd.

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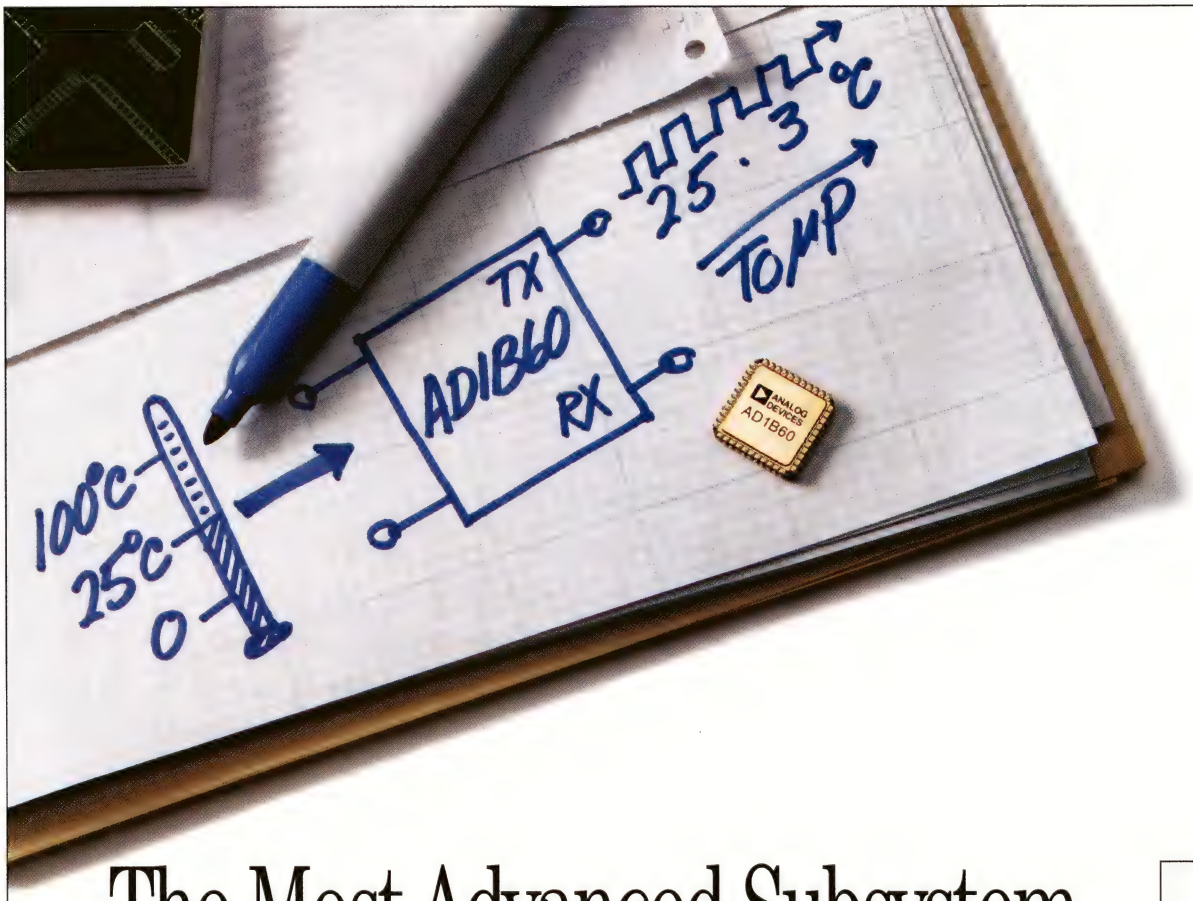
CIRCLE NO. 73



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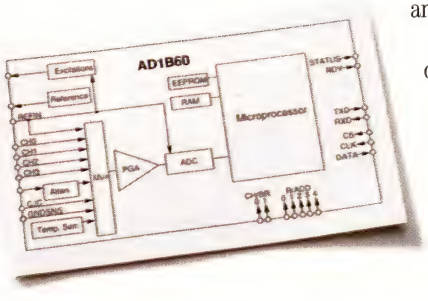
We'll send you a datasheet on the AD1B60 and a brochure detailing our full line of industrial components.



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- **Configurable inputs**
- **Max error of 0.2°C over temp. range**
- **Linearized serial output**

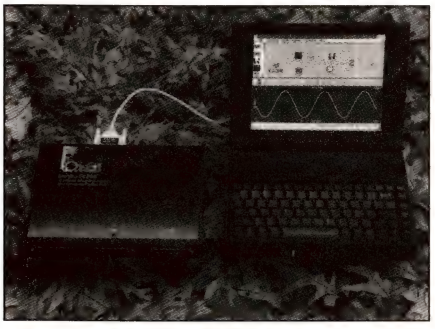
ANALOG DEVICES

Analog Devices, Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106.

CIRCLE NO. 65

waves and TTL/HCMOS signals whose frequency is accurate to within 5 ppm. Phase noise is <–90 dBc at a 1-kHz offset. Spurious signals are <–45 dBc, and harmonics are <–40 dBc. Output amplitude is 12V p-p into an open circuit. An attenuator reduces the output up to 70 dB in 10-dB steps. An accompanying C program, which runs under DOS, lets you set attenuation and frequency. The program can sweep the output through various settings and dwell at points you choose for programmable intervals. $399. **Novatech Instruments Corp,** Seattle, WA. (206) 328-6902. **Circle No. 357**

Logic-analyzer probe minimizes wiring messes. Using a 24-in. controlled-impedance cable, the $395 ActivCable provides a high-density, high-impedance, >200-MHz-bandwidth connection to logic-analyzer probes or a breakout box from a 48-point connector. The connector occupies <0.5 in.^{2} on a board. Active circuits in the cable hold the loading on any line to 4 pF and 30 µA. The circuits draw no power from your board and allow you to set separate threshold voltages (–5 to +5V) on two groups of 24 channels. The $1950 breakout box terminates as many as 192 signals. **Biomation Corp,** Milpitas, CA. (408) 435-7800. **Circle No. 358**



I/O unit for notebook PCs communicates at 500 kbytes/sec. The 8½×11×1⅜-in. DaqBook/200 connects to a PC via a bidirectional enhanced-parallel-port (EPP) interface that also works with standard parallel ports. The unit, whose ADC resolves 16 bits at 100 ksamples/sec, acquires 16 analog signals (expandable to 256 signals) and includes 16 high-speed digital inputs, 24 general-purpose digital I/O lines, five counter/timers, and two 12-bit DACs. The vendor supplies DOS and Windows drivers for C, Basic, Visual Basic, and Visual C++. With these drivers, the unit emulates several industry-standard ISA-bus data-acquisition cards. $1995. **IOtech Inc,** Cleveland, OH. (216) 439-4091. **Circle No. 359**

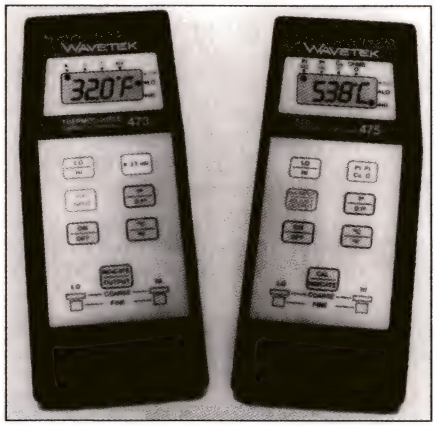
Tools add joint time-frequency analysis to graphical programming system. The $495 Joint Time-Frequency Analysis (JTFA) Toolkit is a virtual-instrument library for the vendor's LabView graphical programming system, which runs on Macintosh and Windows PCs, and Sun SPARCstations. JTFA is a technique for analyzing signals whose frequency content varies over time. For users who do not have LabView, a JTFA executable program, which runs on any computer that can run LabView, reads files of time signals, transforms the signals into the time-frequency domain, and displays the results in a spectrogram. **National Instruments Corp,** Austin, TX. (512) 794-0100. **Circle No. 360**

ISA-bus boards take 2M 12-bit or 1M 14-bit samples/sec. The PC-414F (2M samples/sec/channel, 12 bits, $1995 (one) with 1k-word FIFO) and the PC-414G (14 bits, 1M samples/

sec/channel, $2195 (one) with 1k-word FIFO) include level-sensitive trigger circuits. You set the trigger levels using a 12-bit DAC that also provides an analog output. The units transfer data via the ISA bus or a 10-MHz parallel port that connects directly to many array processors. **Datel Inc**, Mansfield, MA. (508) 339-3000. **Circle No. 361**

$495 ISA bus board acts as autocalibrating 3¾-digit DMM. The autoranging DMM-100 takes as many as 10 samples/sec or waits more than an hour between samples. The board performs alarm-state monitoring and averaging functions. Ready-to use-software for DOS and Windows logs data to disk; the Windows version also graphs acquired data. Drivers allow you to write your own applications in high-level languages. **Quatech Inc**, Akron, OH. (216) 434-3154. **Circle No. 362**

Handheld battery-powered units simulate temperature sensors for calibration. Model 473 ($795) produces an output that simulates that of a type J,



K, or T thermocouple while simultaneously converting the output of a 4- to 20-mA transmitter into a corresponding temperature display. You calibrate a transmitter by supplying it with a simulated sensor output and adjusting the transmitter until its displayed output agrees with its input. Model 475 ($895) performs a similar function, except that it simulates 100Ω platinum or 10Ω copper RTDs. Both units also accept sensor outputs directly and display the corresponding temperature. **Wavetek Corp**, San Diego, CA. (619) 279-2200. **Circle No. 363**

PC-based software simplifies creation and editing of arbitrary waveforms. AnyWave works with the vendor's instruments. The software lets you draw or edit waveforms using a mouse and transfer them to an arbitrary-waveform generator (ARB). You can also transfer the waveforms to the vendor's DSOs for use as templates in comparison testing. The software lets you load and modify waveforms acquired by DSOs, including waveforms acquired by the handheld Scopemeter. $395. **Fluke Corp**, Everett, WA. (800) 443-5853. **Circle No. 364**

225-MHz counter/timer offers optional 2.4-GHz channel. The 10-digit half-rack-size Model 776 ($1995) has two independent channels. Besides a third 2.4-GHz channel, the 776/2.4G ($2495, available spring 1994) includes a temperature-compensated crystal oscillator stable to 0.1 ppm/month. The units incorporate an IEEE-488 interface that transfers 100 ASCII-formatted readings/sec. **Keithley Instruments Inc**, Cleveland, OH. (216) 248-0400. **Circle No. 365**

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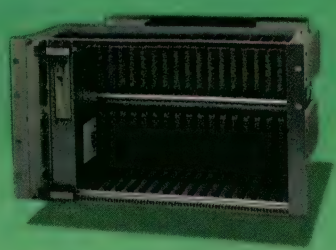

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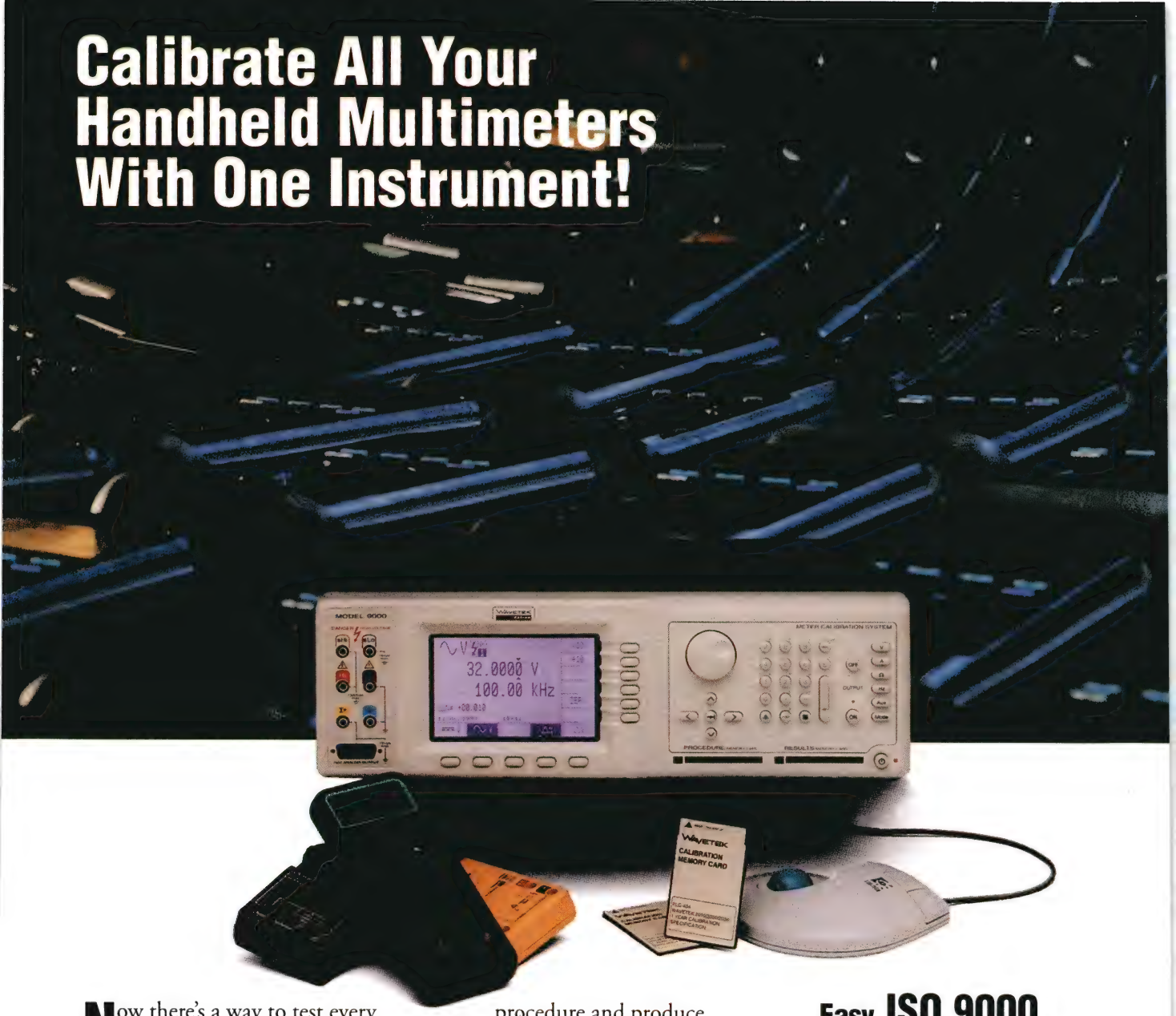
CIRCLE NO. 113

Calibrate All Your Handheld Multimeters With One Instrument!



Now there's a way to test every function of your handheld multimeters quickly, easily, and affordably. That's voltage, current, resistance, capacitance, conductance, temperature—even pulse and logic functions. All fully traceable.

The new Wavetek Model 9000 Multifunction Calibrator not only provides *continuously variable active impedance* and test signals, but can also lead unskilled operators through the calibration procedure and produce certificates of calibration. And it does it in half the time of most other methods!

The fully variable output and "% Deviation" function let you read and record percentage error on every scale of the meter under test. An optional trackball speeds function selection and output setting. Best of all, the Model 9000 can pay for itself in a remarkably short time.

Calibrator Functions	
DC Voltage	±1050 V
AC Voltage	1050 V, 10 Hz - 100 kHz
DC Current	1 µA - 20 A
AC Current	20 µA - 20 A
Resistance	0 Ω - 400 MΩ
Conductance	2.5 nS -2.5 mS
Capacitance	0.5 nF - 40 mF
Frequency	0.5 Hz - 10 MHz
Temperature:	
"K Type" T/C	−250°C - +1350°C
PRT100	−200°C - +850°C
Pulse:	
Duty Cycle	0.05% - 99.95%
Pulse Width	0.30 µs - 1999.9 ms
Logic	TTL, ECL, 5V CMOS

Easy ISO 9000 Certification. With new ISO 9000 directives requiring documented calibration of all test equipment, Wavetek's new Model 9000 Multifunction Calibrator is the solution for all your handheld meters. Now you can meet all these new requirements, test every function of your multimeters, and save calibration time as well.

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CIRCLE NO. 116

WAVETEK

Clock-IC family takes building-block approach

Synergy Semiconductor's SY10xxx/SY100xxx clock ICs

Part No.	Function	Price (1000)
SY10EL34	Clock generator	$7.85 (÷2, 4, or 8)
SY10S834	Clock generator	$8.75 (÷1, 2, or 3)
SY10E111	1:9 differential driver	$15.75
SY10H841	1:4 translating driver	$8.75
SY10H842	1:4 translating driver	$8.75
SY10H843		$8.75
SY10H641	1:9 translating driver	$11.50
SY10H645	1:9 TTL driver	$11.50
SY10H646	1:8 translating driver	$11.50
SY69401	Master/slave clock distribution (150 MHz)	$19.85
SY10E195	2-nsec delay, 20 psec/step	$18.45
SY10E196	Analog-tuned delay line	$19.55
SY89424	1-GHz PLL clock synthesizer	$17.85
SY89429	25- to 400-MHz synthesizer	$18.75

Before high-speed CMOS became available, designers turned to ECL to handle clock frequencies above 10 MHz. Now that circuits run at frequencies above 50 MHz, designers may again want to use ECL in clock distribution, but not just for its speed. ECL's low-voltage-swing differential-I/O interface generates less EMI and is less sensitive to noise than the TTL interfaces of high-speed CMOS. Synergy Semiconductor's ClockWorks ICs offer designers this ECL feature for clock signals and provide a TTL interface to the rest of the circuit.

The family provides a range of product types for clock generation and distribution: frequency synthesizers, clock generators, clock drivers, delay lines, and phase-locked loops. Family members interconnect using positive-referenced ECL (PECL) to reduce noise. They continue using differential signals internally to maintain precise duty-cycle control.

Low-skew TTL interfaces drive the rest of the circuit. All family members have part-to-part skew specified as less than 1 nsec. The SY10/100H842 1:4 driver IC, for example, offers a maximum skew of 400 psec pin-to-pin and 500 psec part-to-part. In addition to low skew, the TTL interfaces provide drive where needed, typically 24 mA.

All ClockWorks family members interconnect without buffers or translators, allowing designers to use a building-block approach to clock-subsystem design while maintaining low skew levels. The SY10xxx parts use 10,000 ECL levels; SY100xxx parts using 100,000 ECL levels are also available.

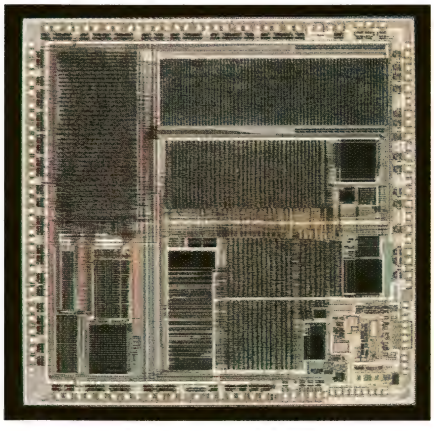
—Richard A Quinnell

Synergy Semiconductor, Santa Clara, CA. (408) 730-1313.

Circle No. 335

Chip replaces Ethernet/SCSI boards

The PCnet-SCSI IC from Advanced Micro Devices is a single-chip replacement for Ethernet and SCSI adapter boards in systems that use the PCI bus. By combining the functions onto a single IC, the device allows designs to offer both capabilities while using only one PCI load. The 132-pin plastic quad flatpack is part of a pin- and software-compatible family of I/O chips for creating multiple-capability, common-design systems.



Combining Ethernet and SCSI functional cores, the PCnet-SCSI offers adapter-board functions with a single PCI load.

The PCnet-SCSI device (Am79C974) is a PCI bus master with two functional cores: SCSI and Ethernet. The SCSI core offers an 8-bit single-ended SCSI-2 interface with a 10-Mbyte/sec data-transfer rate, a DMA with a 96-byte FIFO buffer for burst transfers, and a 32-bit PCI-bus interface. The Ethernet core includes a media-access-control (MAC) unit, an attachment-unit interface (AUI), and a media-attachment unit (MAU) for 10Base-T (twisted-pair) Ethernet. The core is compatible with the Novell NE2100/1500T adapter cards.

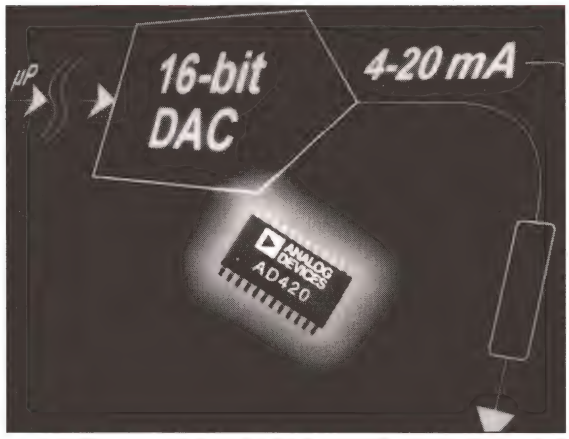
A wide range of software drivers for the device is available for unlimited distribution with a single startup fee. The SCSI drivers include support for Windows 3.1 and NT, MS-DOS 5.0/6.0, IBM OS/2 2.x, and SCO Unix. The Ethernet drivers work with Novell NetWare 2, 3, and 4; Microsoft LANManager, Windows NT, and Windows for Workgroups; IBM LANServer, Artisoft LANtastic, Banyan Vines, and SCO Unix. Advanced Micro Devices maintains and upgrades all drivers.

Two other family members are pin- and software-compatible with the Am79C974 but offer reduced capability. PC-SCSI offers just the SCSI capability, and PCnet-PCI offers just the Ethernet capability. Because the devices are pin-compatible, designers can produce one board design that offers varying capabilities, depending on the parts installed.

The PCnet-SCSI (Am79C974) costs $39.95 (1000). Samples are available now, and the company plans to begin shipping production quantities during the second quarter. The other two devices are also available, and production will begin in the first quarter. The Ethernet-only device, the PCnet-PCI, costs $29.95. The PC-SCSI (Am53C974) costs $24.95.**—Richard A Quinnell**

Advanced Micro Devices, Sunnyvale, CA. (408) 749-5703. **Circle No. 336**

16-bit DAC drives current loops



By directly driving 4- to 20-mA current loops, the 24-pin AD420 replaces a separate DAC and loop-current driver.

The AD420 16-bit DAC from Analog Devices provides a single-chip interface between a µP and industry-standard 4- to 20- and 0- to 20-mA current loops. You can also configure the IC to provide output voltages of 0 to 5V, 0 to 10V, or ±10V using a single external buffer amplifier. The device is available in 24-pin DIP and SOIC packages.

The sigma-delta DAC is monotonic to 16 bits, and has a maximum integral nonlinearity of ±0.006%. You can trim the offset and gain error, which are a maximum of ±0.1% and ±0.2%, respectively, using two external potentiometers. Settling time to 0.1% of full scale is typically 3 msec.

The device supports several processor-interface choices. The serial interface is compatible with both the SPI and MicroWire family of µPs. The DAC also has an asynchronous interface option, which reduces the number of interface wires from three to two. The DAC includes peripheral circuitry, such as a precision 5V reference with a maximum drift of 30 ppm/°C and fault-detection circuitry that warns of an open circuit in the loop.

Additional features include an asynchronous reset to the low end of the range, a 0- to 24-mA overrange capability, the ability to daisy-chain multiple devices using a 3-wire interface, and provision for an external output transistor. Using an external transistor shifts the power dissipation outside the device for high-temperature operation. Typical quiescent current is 3.5 mA; maximum is 4 mA.

The $10 (1000) IC operates from a single power supply between 12 and 36V. Loop compliance is from 0 to within 2.5V of the supply voltage. The operating temperature range is –40 to +85°C.—**Anne Watson Swager**

Analog Devices Inc, Wilmington, MA. (617) 937-1428. **Circle No. 337**

Op amps drive 10,000-pF loads

Linear Technology's LT1354 through LT1365 family of 12 single, dual, and quad op amps use a circuit topology that prevents oscillation with capacitive loads up to 10,000 pF. The circuit topology of these stable op amps—which combines true voltage feedback with the slewing behavior of current feedback—provides them with 400- to 1000-V/µsec slew rates and 1.25- to 7.5-mA max supply currents (see **table**).

As the capacitive load increases of what the company calls its "CLOAD" op amps, both the bandwidth and phase margin decrease, so peaking occurs in the frequency domain and in the transient response. All the amplifiers are unity-gain stable and include specifications for operation from ±15, ±5, and ±2.5V supplies.

Maximum offset voltages range from 0.8 (LT1354/5/6) to 1.5 mV (LT1363/4/5), maximum input bias currents range from 300 to 2000 nA, maximum input offset currents range from 70 to 350 nA, and settling time to within 0.01% of a 10V step ranges from 280 to 80 nsec. Respective specifications for the LT1357/8/9 and LT1360/1/2 amplifiers are within these ranges. The input noise voltage for all amplifiers is between 8 and 10 nV/√Hz.

The amplifier family suits a wide variety of applications—from active filters to video. The two amplifiers of the LT1355 and external components can implement a 100-kHz fourth-order Butterworth Filter. Video specifications of the LT1363 include differential gain and phase of 0.06% and 0.04°, respectively.

Prices range from $2.25 and $2.50 for the single LT1360 in 8-pin DIP and SOIC packages, respectively, to $6.80 and $7.35 for the quad LT1359 in 14-pin DIPs and SOICs, respectively (1000). Samples are available.—**Anne Watson Swager**

Linear Technology Corp, Milpitas, CA. (408) 432-1900. **Circle No. 338**

Linear Technology's high-speed op amps

Part No. (single/dual/quad)	Gain bandwidth (MHz)	Slew rate (V/µsec)	Supply current (mA: maximum/amp)
LT1354/55/56	12	400	1.25
LT1357/58/59	25	600	2.5
LT1360/61/62	50	800	5
LT1363/64/65	70	1000	7.5

Cache memory fits onto single chip

Developed on a memory-intensive ASIC foundation, Sony's CXK784862Q is the first in a planned family of integrated cache-memory devices for 80x86- and Pentium-based computer systems. The 160-pin device contains a complete level-two cache-memory subsystem, including memory, a controller, and tag RAM.

The device provides a 256-kbyte, 2-way set-associative cache. Its main memory is organized as two 32k×36-bit memory blocks. It also includes two 4k×20-bit tag RAMs and a cache controller. The memory uses a write-through protocol and is designed for connection to 486 logic-core chip sets.

The cache subsystem chip comes in 33- and 50-MHz speeds. It operates in a look-aside configuration, allowing burst access (2-1-1-1) with zero-wait-state performance. You can cascade chips to form cache subsystems as large as 1 Mbyte that offer the same performance as the basic device.

The CXK784862Q comes in a 160-pin plastic quad flatpack and uses less than 2W when operating at 50 MHz. Samples, $125 (100); OEM qty, <$100 (5000).—**Richard A Quinnell**

Sony Component Products Company, Cypress, CA. (800) 288-7669. **Circle No. 339**

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Maxim's industry-leading MAX782/MAX783/MAX786 dual-output 3.3V & 5V notebook power supplies provide:

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  - 25µA $I_{SHUTDOWN}$ (MAX783/MAX786)
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  - 300kHz master oscillator
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  - Dual PWM, 3.3V and 5V buck regulators
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  - Precision voltage monitors
- **Lowest Noise and EMI:**
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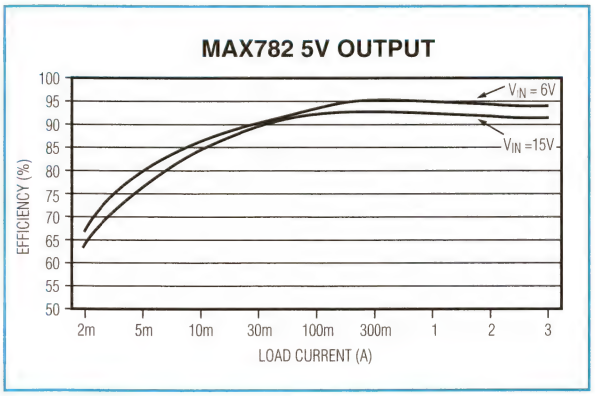
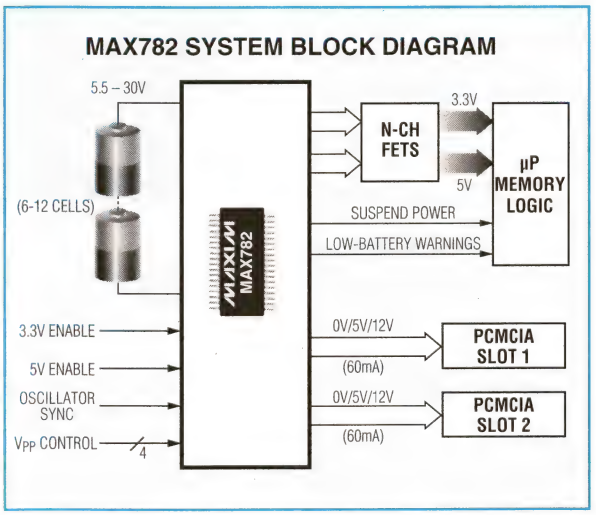
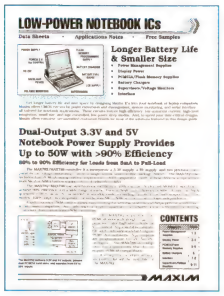
  - Fixed-frequency for noise-sensitive RF-wireless systems

MAX782 and MAX783 are $5.95*, and the MAX786 is $4.15*. For quick evaluation, order a pre-assembled demo board (order MAX782EVKIT-SO, MAX783EVKIT-SO, or MAX786EVKIT-SO).







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CIRCLE NO. 93

INTEGRATED CIRCUITS

ATM chip set handles 622 Mbps. Comprising three ICs and a multichip module, the PM53xx ATM chip set implements the physical-layer interface for SONET and SDH transmission media. The set includes the PM5312 transport-terminating transceiver ($170), the PM5318 serial-to-parallel conversion chip ($120), the PM5345 Saturn user-network interface ($47.60), and the PM5712B SONET line interface ($1100). **PMC Sierra**, Burnaby, BC, Canada. (604) 688-7300. **Circle No. 418**

Step-down controller provides 7A. The MAX767 controller converts a fixed 5V supply to a 3.3V output at up to 7A without a heat sink. Because of a 300-kHz operating frequency, the device is very small. It also features low-cost external components, including all n-channel construction in the application circuit. All n-channel construction and synchronous rectification result in 90% efficiency over a wide range of load conditions. The quiescent power of 750 μA drops to 125 μA in standby mode. In 20-pin shrink SOP packages, the device costs $3.40 (1000). **Maxim Integrated Products**, Sunnyvale, CA. (408) 737-7600. **Circle No. 419**

20-bit DAC has –96-dB distortion. The PCM1702 audio DAC features –96 dB max THD plus noise, 104-dB typ dynamic range, 110-dB typ S/N ratio, 200-nsec typ settling time, and 150-mW typ power dissipation. In a 16-pin DIP or 20-pin SOP, the $17.08 (100) device operates from –25 to +85°C. **Burr-Brown Corp**, Tucson, AZ. (800) 548-6132. **Circle No. 420**

Analog engine conditions instrumentation signals. The 4301 IC combines three general-purpose op amps with characteristics in the 4558 class, an exponentially controlled voltage-controlled amplifier, and a log-responding rms-level sensor. The IC permits remote programming of front-end gain while sensing true-rms signal levels. The dynamic range is 115 dB, and THD does not exceed 0.01% at unity gain. In a 20-pin DIP or 24-pin surface-mount package, the device operates up to 75°C. $4.39 (1000). **That Corp**, Marlborough, MA. (508) 229-2500. **Circle No. 421**

10-bit CMOS ADC converts 40M samples/sec. The SPT7860 is part of a family of 10-bit CMOS ADCs that range from 5 to 40M samples/sec. All of the converters feature differential linearity of ±1/2 LSB, integral linearity of ±1 LSB, and guaranteed no missing codes. S/N ratio is 56 dB at an input frequency of 1 MHz. Power dissipation ranges from 75 mW for the 5M-sample/sec 7835 to 200 mW for the 7860. The converters feature on-chip T/H amplifiers and input capacitances of 5 pF. In 28-pin DIPs and SOICs, the devices cost $9.60 to $43.50 (1000). **Signal Processing Technologies Inc**, Colorado Springs, CO. (719) 528-2314. **Circle No. 422**

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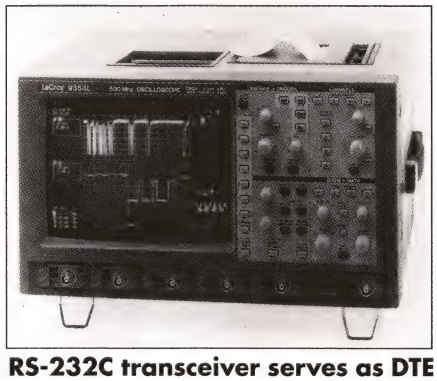

RS-232C transceiver serves as DTE or DCE ports. The MAX214 programmable 5V RS-232C contains three drivers and five receivers. A control pin programs the device as an 8-line serial port for data-terminal and data-circuit equipment (DTE and DCE). Dual charge pumps, operating with 1-μF external capacitors, generate the voltage to produce minimum ±5V transmitter-output levels. Data rates are as high as 116 kbps. A shutdown mode reduces the quiescent supply current from 20 mA to 20 μA. $3.99 (1000). **Maxim Integrated Products**, Sunnyvale, CA (408) 737-7600. **Circle No. 423**

Fax and voice chip suits portable applications. The 73D2950 datafax/voice chip set integrates the transformerless Data Access Arrangement (DAA). An optional T version uses the TrueSpeech audio-compression algorithm, which the company recently licensed with the DSP Group. The 3-chip set includes a microcontroller, the DSP, and an analog front-end line-interface circuit. The set and associated RAM, ROM, and DAA components consume <150 mW of power. The components suit 3.3 and 5V systems and incorporate power-down features. The set costs around $22 (OEM); T version, $29.50. **Silicon Systems**, Tustin, CA. (714) 573-6200. **Circle No. 424**

Video RAMDAC incorporates clock generators. The ICS5340 merges a triple 8-bit video DAC with a color-palette RAM and two timing generators. The device handles 24-bit color through 8-bit pseudocolor at clock rates to 135 MHz. Its timing generators provide a selection of eight video clocks and two memory clocks. Samples and demonstration boards are available. Prices begin at $6.95 (50,000). **Integrated Circuit Systems Inc**, Valley Forge, PA. (215) 630- 5300. **Circle No. 425**

Op-amp outputs swing rail to rail. The TLC2262 and TLV2262 single-supply op amps consume 0.4 mA. The C2262 operates from one 5V supply or up to a ±8V supply. The V2262 works best on 3V systems but also runs off 5V systems. Typical noise at 1 kHz is 12 nV/√Hz, and input-bias current is typically 1 pA. Both op amps are available in DIP, SOIC, and thin-shrink SOP packages. The SOP package occupies half the space of a standard surface-mount SOIC package. In DIPs, the TLC2262 and TLV2262 cost $0.82 and $0.99 (1000), respectively. **Texas Instruments**, Denver, CO. (800) 477-8924 ext 4500. **Circle No. 426**

Gate array addresses military needs. The FX150KM gate array has more than 150,000 raw gates and 256 signal I/O pins. The vendor manufactures the chip in a 0.6-μm H-GaAs III process featuring a sea-of-gates architecture. Typical gate delays are 60 psec, and gate power dissipation is 0.18 mW unloaded. The device withstands dose radiation >100 MRADs. The arrays comply with MIL SPEC 883-C standards and cost $0.005 to $0.03/gate. **Vitesse**, Camarillo, CA (805) 388-3700. **Circle No. 427**

Quad analog switch matches on-resistance. The MAX333A CMOS IC has four independent switches with 35Ω max on-resistance, 2Ω matching between the channels, and 5Ω variation over the analog signal range. Charge injection is less than 5 pC, ESD tolerance is greater than 2000V, break-before-make action is typically 10 nsec, and turn-on and -off times are less than 175 and 145 nsec, respectively. Quies-

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- **4 Serially Programmed Digital Outputs for Remote Control of MUX/PGA**
- **±10pA Input Current**
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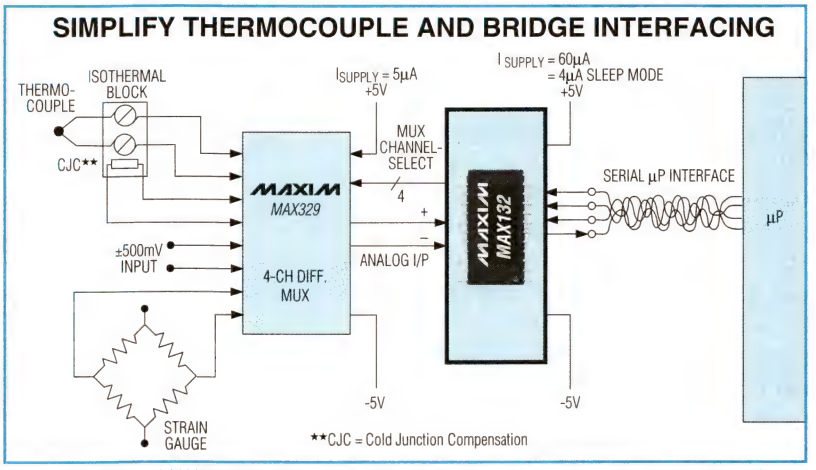
- **Parallel Interface Version Available – MAX135**



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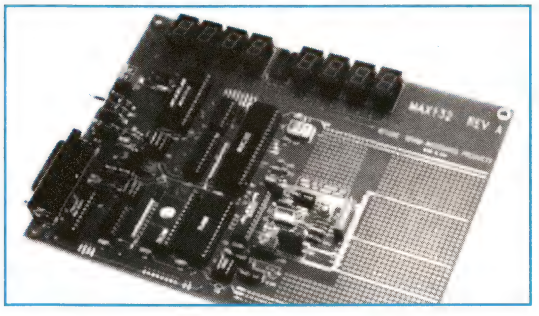

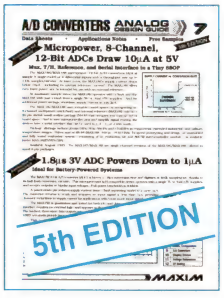

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CIRCLE NO. 94

Xicor®

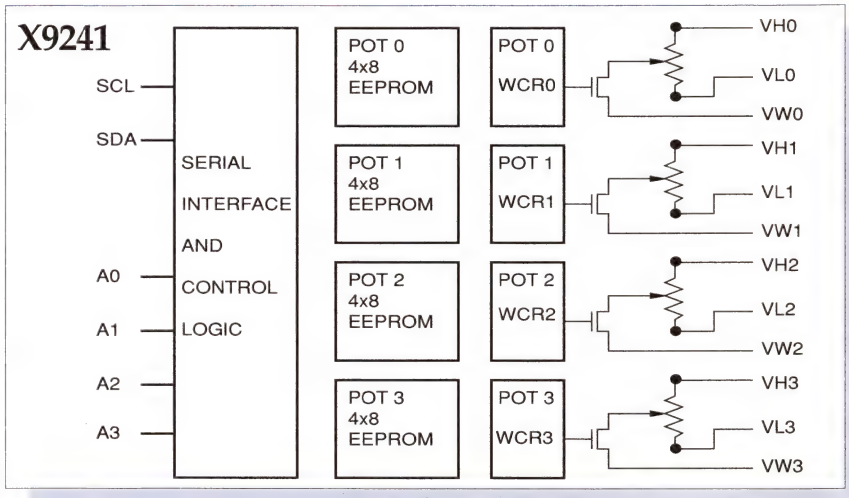
#2
Q1/93

Design Engineers Bulletin

New Product and Applications Information for Design Engineers

Xicor's New X9241 Quad Potentiometer Allows Factory Automation of 64 Potentiometer Adjustments via a Digital Two Wire Serial Bus

For complex systems requiring multiple adjustment capability, Xicor offers the new X9241, Quad E²POT. In addition to retaining wiper positions without power, the X9241 offers a two-wire serial interface for controlling the potentiometers independently or simultaneously using microprocessor control commands. A user programmable address allows up to 16 devices to be software controlled via the common two wire serial bus.



QUAD E²POT Development System

PC based system automates production adjustments of system potentiometers

The XK9241 can be used in a production environment to optimize the settings of the E²POT.

Faster analog circuit checkout and calibration is made possible by Xicor's new XK9241W Quad E²POT Development System. This system consists of an X9241 evaluation board, interface cables and software which allows a design engineer to control all functions of the Xicor X9241 Quad E²POT from a menu driven system on a IBM PC Compatible computer. The XK9241W Development System allows the design engineer to place the X9241 in a target analog system and perform all adjustments and configuration needed to recognize the features and benefits of the Quad E²POT. The XK9241 PC based development system can also be used in production environments to automate potentiometer adjustments for initial system calibration.

The XK9241 supports all versions of the X9241 family. It can simultaneously control up to 16 different Quad E²POTs on the same two-wire bus to effectively allow adjustment of 64 individual E²POTs. Orders for the XK9241W can be placed with any authorized Xicor distributor. Suggested resale price is **$188.00.**

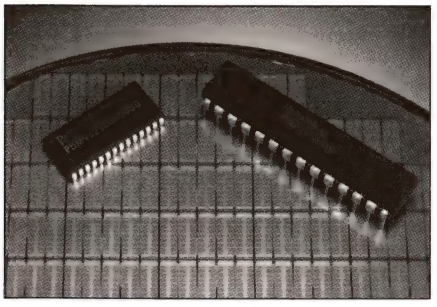
Xicor Inc., 1511 Buckeye Drive, Milpitas, CA 95035 Fax (408) 432-0640 Tel (408) 432-8888

cent power consumption is 35 μA. Price starts at $3.46 (1000). **Maxim Integrated Products**, Sunnyvale, CA. (408) 737-7600. **Circle No. 428**

Interface IC handles scanner image sensors. The M62490FP works with contact image sensors and CCDs, converting the analog scanner signals to digital. It includes ADC, S/H, gain-control, and black-level-control circuits on chip, offering an 8.5-dB gain with a 5-MHz bandwidth. The 42-pin device costs $3.50 (10,000). **Mitsubishi Electronics America**, Sunnyvale, CA. (408) 730-5900. **Circle No. 429**

Palette DACs operate as fast as 250 MHz. The RGB series of palette DACs comes in 170- and 250-MHz speeds. The RGB561 ($103, $194) handles 1600×1280×27-bit images with overlay and independent gamma correction. The RGB530 ($71, $116) includes 8-bit overlay and underlay with 24-bit color. The RGB525 ($52, $83) uses pixel packing to achieve 1280×1024×24-bit color with 4 Mbytes of VRAM. **IBM Microelectronics**, Hopewell Junction, NY. (800) 426-0181. **Circle No. 430**

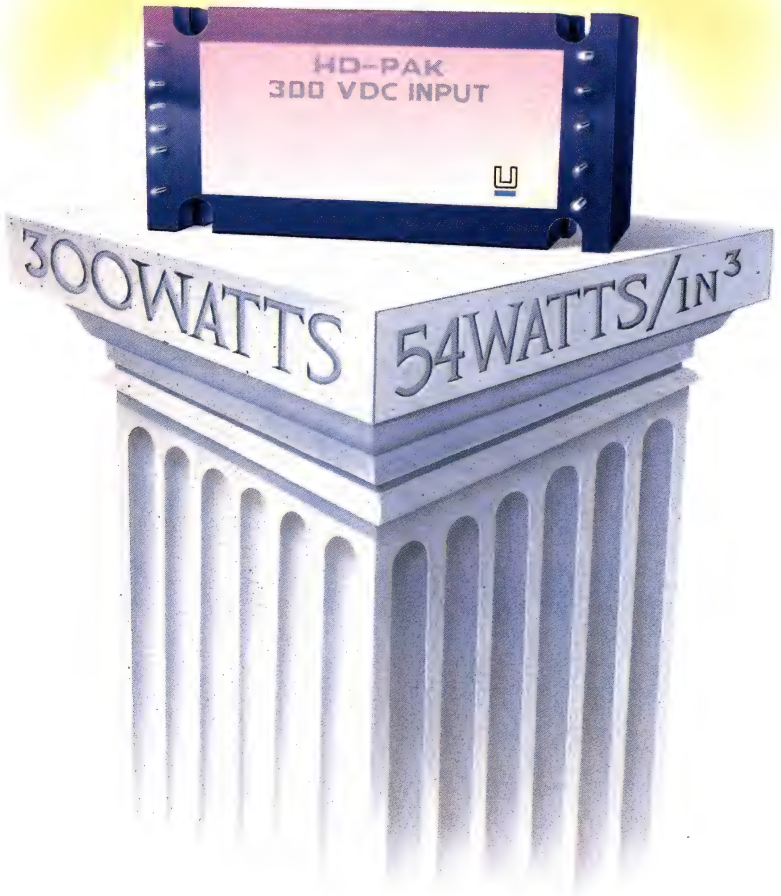
Stereo codecs offer reduced-cost options. Alternatives to the AD1848 codec standard in Windows Sound System audio cards, the AD1846 and AD1847 feature lower cost than the Windows cards. The 1846 is pin and register compatible with the 1848 but has reduced dynamic range (70 dB). The 1847 offers a serial interface to reduce pin count from 68 to 44 pins. Production will begin in March, and prices will be $8 and $7.50, respectively. **Analog Devices**, Norwood, MA. (617) 329-4700. **Circle No. 431**



256-kbit SRAMs have 10-nsec access time. These 256-kbit CMOS SRAMs, additions to the vendor's Paramount series of SRAMs (part no.'s PDM4151SA10, PDM41256SA10, PDM41257SA10, PDM41258SA10, and PDM41298SA10), feature a 10-nsec access time. Three of the devices have 64k×4-bit architectures. The other two offer organizations of 32k×8 and 256k×1 bits. The 64k×4-bit PDM-41298SA10 features an output-enable pin. The 5V parts have an active current of 135 mA and a standby current of 2 mA. Prices range from $11.25 to $12.10 (100). **Paradigm Technology Inc**, San Jose, CA. (408) 954-0500. **Circle No. 432**

Self-timed SRAM has 10-nsec access time. The CXK77910A family of self-timed SRAMs has a 10- or 12-nsec access time. The SRAM can act as cache memory in Pentium and RISC SPARC μPs. The SRAM has a 128k×9-bit organization, and an external clock triggers input and output registers. The chip comes in a TSOP or SOJ package and has a 945-mW power consumption. $100 (100). **Sony Corp of America**, Cypress, CA (714) 220-9100. **Circle No. 433**

Stands Alone



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CIRCLE NO. 101

POWER SOURCES

Quad-output 100W switchers measure 5×3.3×1.5 in. The US100 series quad-output 100W switchers accept 90 to 264V-ac inputs. The units have onboard FCC class B and VDE class A line filters. Each of the four outputs is available in voltages ranging from ±2 to ±48V. (Modifications take three weeks.) Multiple-output models, $93 (100). **Digital Power,** Fremont, CA. (510) 657-2635. **Circle No. 561**

8W converters run for 1 million hours. The 800 series of 8W dc/dc converters offer 1000V-dc isolation and 2:1 input-voltage ranges. The units measure 1×2×0.375 in. Models are available in single-, double-, and triple-output versions. The converters have remote-on/off and converter-synchronization pins. Line- and load-regulation specs are ±0.2%. All units undergo a 72-hour burn-in under a cycled load. Prices range from $58.80 to $66.50 (100). **Conversion Devices Inc**, Brockton, MA. (508) 559-0880. **Circle No. 562**

200W dc/dc converter accepts 300V input. The BASIX dc/dc converters meet VDE0871 Class A requirements without external filtering. Outputs range from 3.3 to 48V. The units measure 4.6×2.4×0.5 in. $160 (OEM quantities). **Computer Products/Power Conversion America**, South Boston, MA. (617) 268-1170. **Circle No. 563**

Regulated 14W dc/dc converters have 4:1 max-input range. The KWX series dc/dc converters accept 9 to 36V or 20 to 72V inputs. Regulated outputs span 5 to ±15V dc. The units measure 3×2.56×0.83 in. $53 (100). **Polytron Devices**, Paterson, NJ. (201) 345-5885. **Circle No. 564**

External supply meets medical specs. The MED 115 external supply meets UL 544. The supply outputs 5V at 0.75A and ±15V at 0.25A. Input is via a hospital-approved line cord, and output is via a 6-ft. cable and DIN connector. $40 (OEM quantities); delivery, stock to 10 weeks ARO. **Elpac Power Systems**, Irvine, CA. (714) 476-6070. **Circle No. 565**

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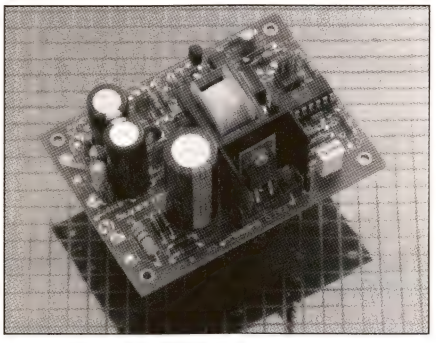
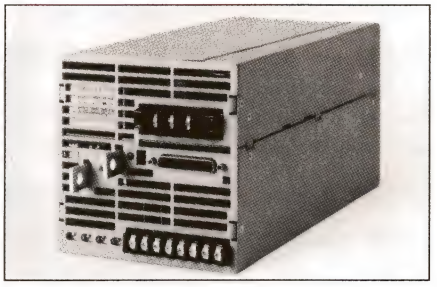
Rectifier blocks withstand 5- to 30-kV pk reverse voltages. The 3HG series rectifier blocks handle currents from 2 to 5A. The blocks are available in half-wave, positive and negative center-tap, and doubled configurations. Resistance- and capacitor-compensated blocks are also available. A 20-kV, 2.25A unit costs $62 (25). **HV Components Associates Inc**, Farmingdale, NJ. (908) 938-4499. **Circle No. 566**

5W dc/dc converters meet MIL-H-38534 Class B. MSA series dc/dc converters measure 1×1×0.27 in. The units handle continuous input voltages from 16 to 40V and meet the power-bus-surge standards of MIL-STD-704A through E. Outputs range from 5 to ±15V. $630 (100); delivery, stock to six weeks ARO. **Interpoint**, Redmond, WA. (206) 882-3100. **Circle No. 567**



Demo board exercises power-supply-controller IC. The model HV9120DB-1 demo board comes with an information packet and an application note explaining the company's PWM switching-supply controller ICs. The demo board is a functional high-voltage off-line supply. $95. **Supertex Inc**, Sunnyvale, CA. (408) 755-0100. **Circle No. 568**

1000W supply sets outputs at factory. You can instruct the company to set the secondary outputs of the



PM3386B multiple-output power supply to any voltage between 2 and 24V dc. As many as five secondary outputs are available. The supply's main output provides 750W at 5 or 24V dc. The supply measures 5×5×11 in. The unit corrects its input-power factor to 0.99% and accepts 96 to 264V-ac inputs. Line and load regulation for the main output are ±0.25%, and ripple and noise are 50 mV p-p. $1095 (small quantities); delivery is from stock. **Pioneer Magnetics**, Santa Monica, CA. (310) 829-6751. **Circle No. 569**

Solid-state fuse carries 4A. The CS310 solid-state fuse trips in microseconds. Units having voltage ratings as high as 30V are available. You reset the unit by killing power. $4.53 (1000). **Inresco**, Manasquan, NJ. (800) 684-6330. **Circle No. 570**

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Computer-input device conveys 3-D position and orientation

The Immersion Probe, a penlike stylus mounted on a lightweight mechanical linkage, provides 3-D information to a computer. You hold the stylus like a pencil and move it freely in 3-D space. The device conveys 3-D position (x, y, and z) and orientation (roll, pitch, and yaw) via a standard serial port. Applications include 3-D CAD, graphic design, digitizing 3-D objects, and 3-D virtual-reality interfaces.

The mechanical linkage supports the stylus, reducing operator fatigue during extended use. The linkage also provides physical resistance, to improve control of fine motions. The self-calibrating device uses mechanical sensor elements that do not suffer from the noise, interference, or shadowing problems of magnetic and ultrasonic tracking devices.

Immersion Probe provides 3-D position and orientation information to a computer via a serial port.

Immersion Probe is available in two models, IC and IX, which vary only in precision. IC measures with 0.05-in. accuracy in a central region and with 0.10-in. accuracy in outer regions; IX improves those figures to 0.025-in. and 0.05-in. accuracy, respectively. Angular resolution of the IC version is 0.7°; with IX, it's 0.3°. IC costs $999; IX is $1495. A developer's programming library—for Macintosh, PC, or SGI systems—sells for $139.—**Gary Legg**

Immersion Corp, Palo Alto, CA. (415) 960-6882. **Circle No. 401**

Rewritable optical disk boosts storage capacity. The 3.5-in. RMD-5300-S magneto-optical disk drive reads and writes ISO-standard 128-Mbyte cartridges and proprietary 256- and 384-Mbyte cartridges. The drive senses which type of cartridge you insert. Sustained data rate is as high as 1.528 Mbytes/sec, and average seek time is 35.2 msec. <$1000 (OEM). **Mass Optical Storage Technologies Inc**, Cypress, CA. (714) 898-9400. **Circle No. 402**

CD-ROM drive doubles speed. The CDU-33A entry-level addition to the vendor's line of double-speed CD-ROM drives reads multisession disks. Thus, it is compatible with Kodak's Photo CD format, and it can play audio CDs. Average access time is 320 msec; sustained data-transfer rate is 300 kbytes/sec. $200. **Sony Electronics Inc**, San Jose, CA. (800) 352-7669. **Circle No. 403**

Transceivers support FDDI over twisted pairs. The PE-6852X series of 100-Mbyte/sec TP-PMD transceivers supports FDDI over data-grade, unshielded, twisted-pair copper wire. MLT-3 encoding and data scrambling control EMI, and adaptive equalization compensates for signal distortion caused by varying cable lengths (to 100m). $40 (1000). **Pulse Engineering Inc**, San Diego, CA. (619) 674-8100. **Circle No. 404**

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Wireless data link connects computer equipment. A pair of transceiver units known as Comrad enable a computer to communicate wirelessly with another computer or with peripheral equipment. The units connect to RS-232C ports and operate on the 900-MHz radio band. No FCC license is necessary. $429.95. **Communications R&D Corp**, Indianapolis, IN. (317) 290-9107. **Circle No. 405**

Tiny video system transmits long distances. The PC-7 video system, which comprises three small boards and a 2.7-oz color video camera, fits in small spaces and can transmit without wires as far as 10 mi. The boards are connected by flexible ribbon cable and can be arranged in different configurations. The smallest configuration is a 2.25-in. cube. Camera, $370; transmitters start at $50. **Supercircuits**, Austin, TX. (512) 335-9777. **Circle No. 406**

Solid-state disk holds 536 Mbytes. The MegaRam-35 solid-state disk stores as much as 536 Mbytes in a 3.5-in. form factor. It transfers data at 10 Mbytes/sec via its SCSI-2 interface, and its access time is 35 µsec. An RS-232C port allows diagnostic testing. Price depends on capacity—approximately $100/megabyte. **Imperial Technology Inc**, El Segundo, CA. (800) 451-0666. **Circle No. 407**

Stereo displays boost brightness and contrast. Two 19-in. color stereo displays provide higher contrast and brightness than earlier models. The SGS19U works with normal vertical sync or external frame sync; the SGS19C works with stereo-ready workstations or computers that provide a 50- to 152-Hz frame sync signal. Both have a liquid-crystal modulator and work with passive stereo glasses. $8995 each. **Tektronix Inc**, Wilsonville, OR. (800) 835-9433, ext 5000. **Circle No. 408**

Digitizer works with touch or pen. The TouchPen digitizer provides both touch and pen input for flat-panel displays. It draws 60 mA while operating and 2 mA in sleep mode. $795. **MicroTouch Systems Inc**, Methuen, MA. (508) 659-9000. **Circle No. 409**

Touchscreen controller fits on half-sized PC card. The E281-4035 touchscreen controller fits on a half-sized card for the ISA or EISA bus. Touch-response time for a 19-in. monitor is 22 msec. Onboard diagnostics test the

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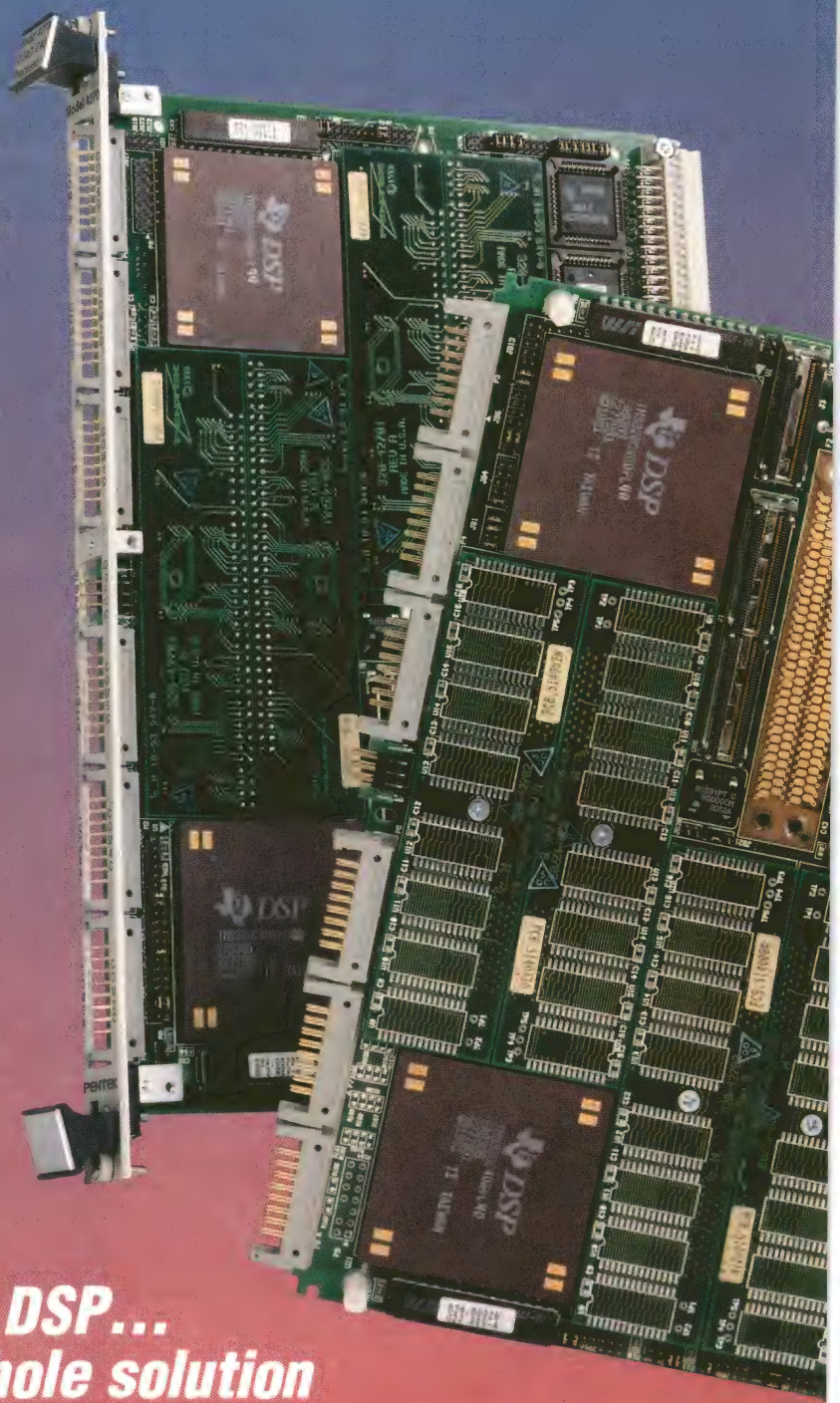

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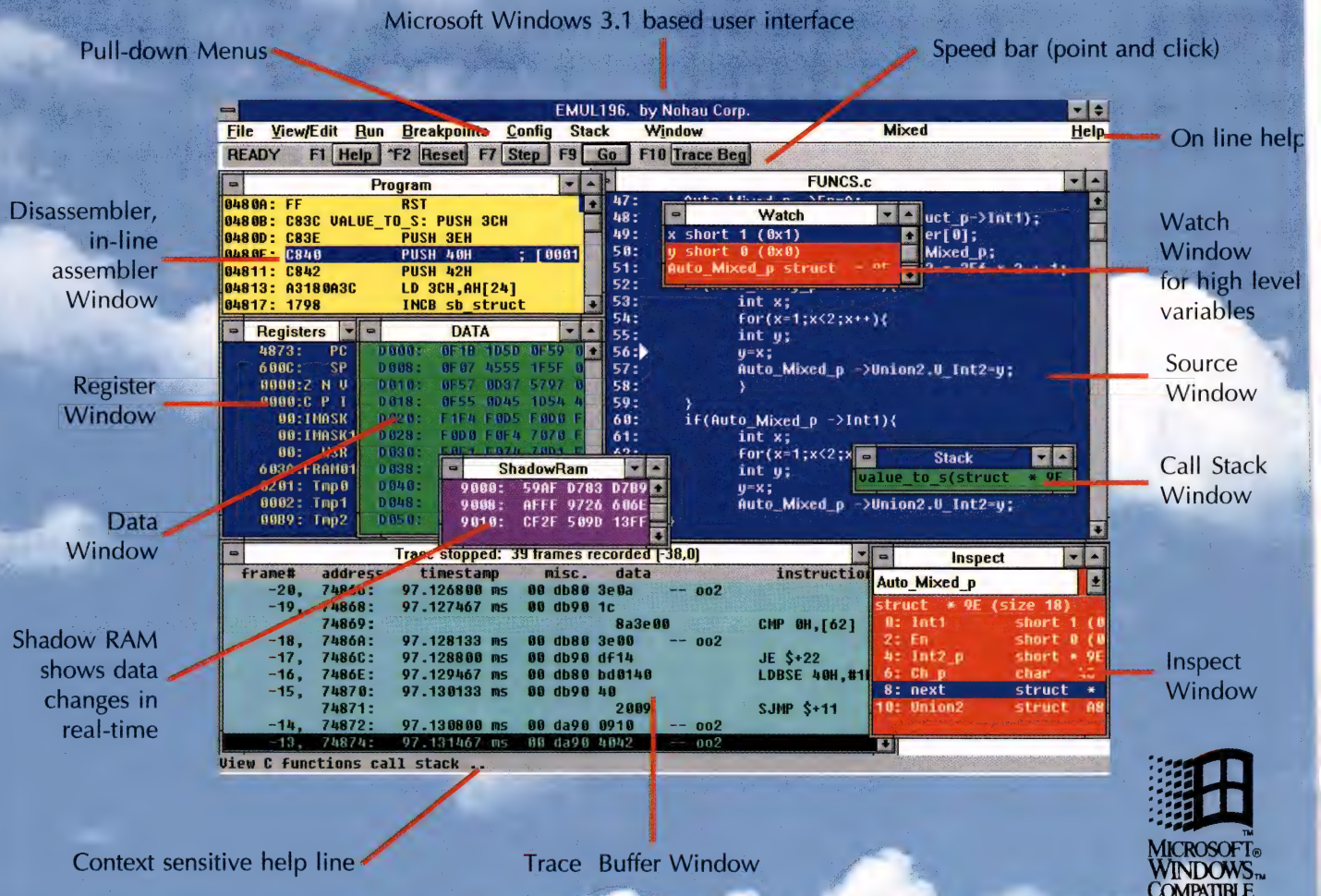

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CIRCLE NO. 98

touchscreen, controller, and cabling. From $255. **Elographics Inc**, Oak Ridge, TN. (800) 868-6824. **Circle No. 410**

X terminals lower entry-level cost. The ECX series of color X terminals perform better and cost less than their predecessor models. Three models—with 1024×768 resolution in 14-, 15-, and 17-in. monitors—perform at 52,000 Xstones. Prices, respectively, are $1795, $1995, and $2595. **Network Computing Devices Inc**, Mountain View, CA. (415) 694-0650. **Circle No. 411**

Touch frame fits flat-panel displays. The Modular/1LP touch frame mounts on all 200×150-mm flat-panel displays, including many from Hitachi, Panasonic, Sharp, and Toshiba. The device includes a sealable scanning IR screen with circuitry that compensates for water, dust, and airborne particulates. The unit is available with a software- or hardware-based controller, a PC/104 controller, or an RS-232C controller. $380. **Carroll Touch**, Round Rock, TX. (512) 244-7040. **Circle No. 412**

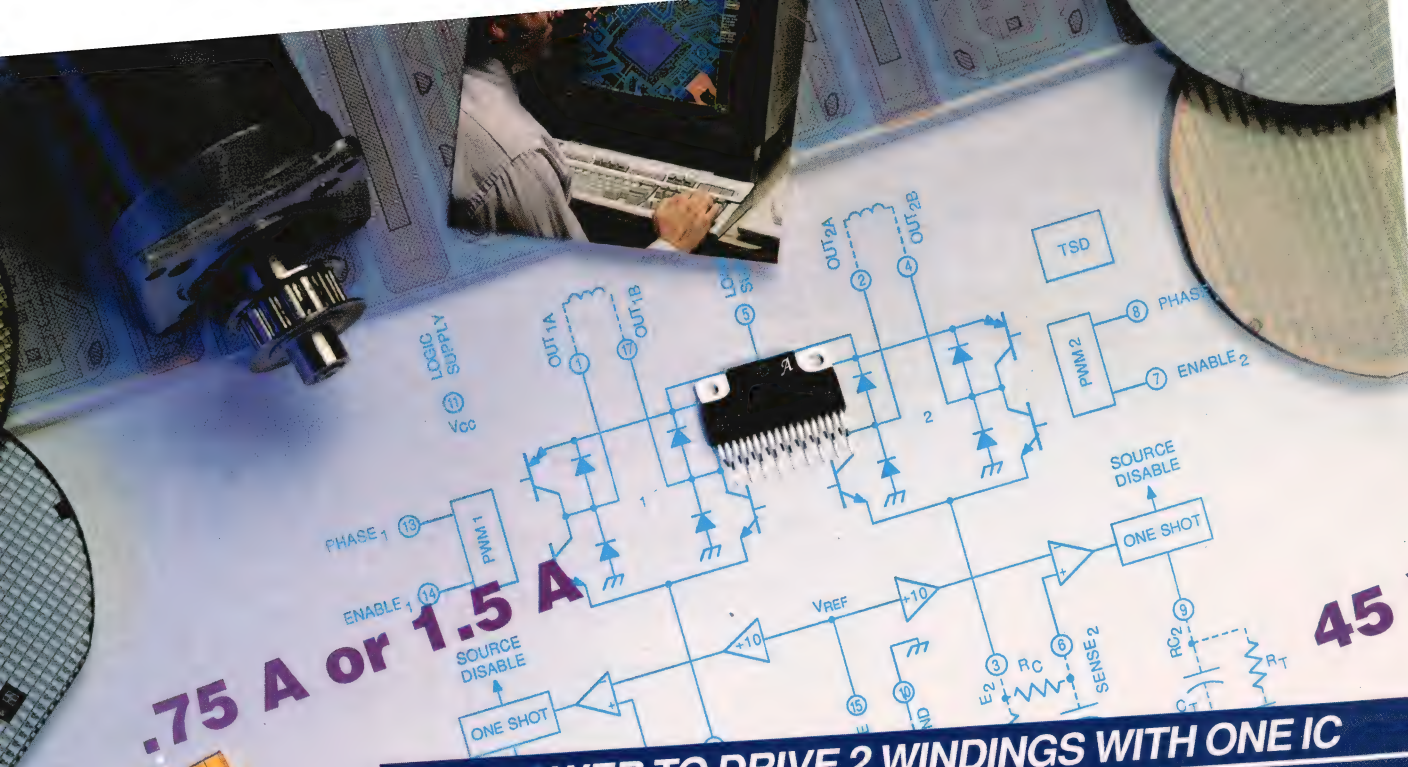
ISA parallel interface meets MIL specs. The NTDS-4610, an NTDS/AT half-length adapter for ISA-bus systems, complies with MIL-E-16400/MIL-STD-2036 and MIL-STD-1397B standards. It features stress screening and conformal coating; it can operate in all four Naval Tactical Data Systems parallel environments. $4589. **S T Research Corp**, Newington, VA. (703) 550-7000. **Circle No. 413**

Flat-panel VGA monitor is useful in hospitals. The ELM-VGA electroluminescent flat-panel display suits hospital information and point-of-care systems. The 10-in. display is 2.7 in. thick; it can mount on a wall, a desk stand, or a bedside swing arm. Users can view its monochrome images from any angle. $1395. **Planar Systems Inc**, Beaverton, OR. (503) 690-1100. **Circle No. 414**

Pocket-sized book is PC reference. The 94-pg *PC Technical Source Book* provides a quick-reference compendium of the most commonly needed facts and figures from myriad PC hardware and software manuals. Contents include diagnostic error codes, CPU summaries, XT and AT add-on card dimensions, BIOS entry points, DOS keystrokes, keyboard scan codes, and ASCII control codes. Free. **Industrial Computer Source**, San Diego, CA. (619) 271-9340. **Circle No. 415**

SBus card lowers graphics cost. The TGX260 graphics frame buffer for the SBus accelerates 2- and 3-D vector rendering for a lower price than Sun products, according to the manufacturer. The single-slot, 8-bit-color, double-buffering card is compatible with all SPARC workstations. It has programmable resolution and refresh rates as high as 76 Hz for 1024×768 resolution. $3495. **Integrix Inc**, Newbury Park, CA. (805) 375-1055. **Circle No. 416**

PCMCIA card holds SCSI controller. The SCSI2GO PCMCIA Type II card contains a SCSI controller. An interface cable to the 16-bit device provides a 50-pin SCSI-2 connector. Supplied software automatically reconfigures your system when you plug the card into a PC. $329. **Future Domain Corp**, Irvine, CA. (714) 253-0400. **Circle No. 417**



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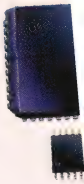

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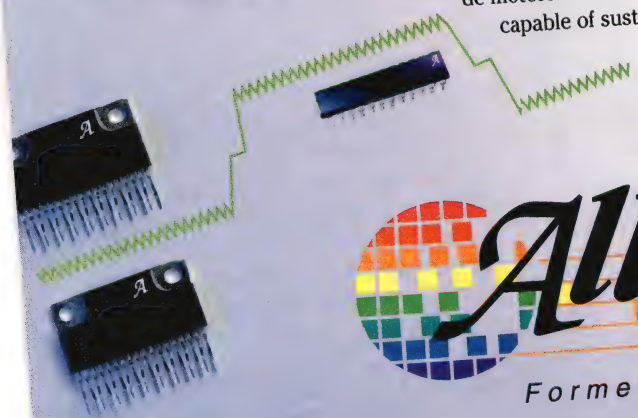

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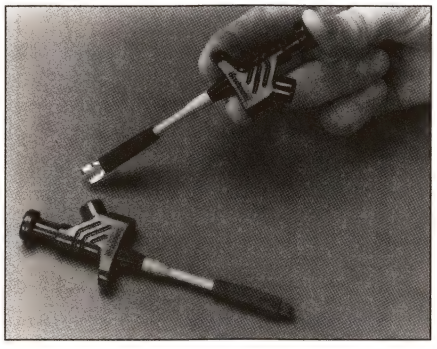
R-2R network is integrated. The IPEC R-2R precision resistor network combines 16 resistors in the usual ladder configuration. The unit comes in 25- or 50-mil pitch, surface-mount packages. Standard values are 10, 25, and 50 kΩ. $1.35 to $2. **California Micro Devices Co**, Milpitas, CA. (408) 263-3214. **Circle No. 368**

Right-angle LEDs are surface mountable. The SIDELED right-angle, surface LEDs come in hyper red, super red, orange, yellow, blue, green, and pure green. The units are 4 mm high. Two emitter versions and one phototransistor version are available for IR applications. $0.24 to $1.82 (1000). **Siemens Components Inc**, Cupertino, CA. (408) 297-7910. **Circle No. 369**

Heat-resistant compound fills many electronics niches. You can mold the Flamehold heat-resistant compound into prototype heat sinks. The compound also replaces machined fixtures during prototype production runs. The material withstands the heat of wave soldering and holds shields, coils, brackets, and other components in place. The material is dimensionally stable, does not deform or swell under heat, does not soil or corrode parts, and is simple to apply and remove. The compound is safe and nontoxic. You can reuse the material indefinitely by adding water. $30 (5 lb). **Nassau Research Corp**, Aliquippa, PA. (412) 375-3300. **Circle No. 370**

Probe measures surface resistance. The model 850 surface-resistance probe measures point-to-point and point-to-ground resistance to EOS/ESD standards 4.1 and 7.1, NFPA 99, ASTM F150, and applicable DoD standards. The probe weighs 5 lbs and uses a 2.5-in.-diameter, conductive-rubber electrode having 65-durometer hardness. The probe will work with common voltmeters. With it, you can measure floors, mats, workbenches, and a variety of other surfaces. **Electro-Tech Systems Inc**, Glenside, PA. (215) 887-2196. **Circle No. 371**

Test probe grips large test points. The KLEPS 280 test probe has a steel, spring-loaded jaw that opens to 0.86 in. Like its smaller cousin's jaws, this probe's jaws simultaneously extend and



open when operated. The probe accommodates 4-mm banana plugs having fixed or retractable sleeves. Thus, the probe meets DIN VDE 0110 electric-shock requirements for 1000V connection. The probe comes in red or black. KLEPS 280: $19; delivery stock to six weeks ARO. **Richard Hirschmann of America**, Riverdale, NJ. (201) 835-5002, ext 230. **Circle No. 372**

Transistors with integrated bias resistors save space. The MUN 2111/2211 series of transistors has bias resistors, a single transistor, and monolithic-base and base-emitter resistors. NPN and PNP devices are available in SC-59 surface-mount packages. $0.12 (3000). **Motorola Inc, Semiconductor Products Sector**, Phoenix, AZ. (602) 244-3742. **Circle No. 373**

Connector family lowers insertion force. New members of the Micro-Strip family of high-density, controlled-impedance, board-to-board and cable-to-board connectors boast 25% lower insertion forces than previous members of the family offered. The connectors have 40 high-speed signal lines/in. $0.15 to $0.25 per line. **AMP Inc**, Harrisburg, PA. (717) 564-0100. **Circle No. 374**

Heat sinks cool multiwatt devices. Two heat sinks slide onto multiwatt devices, requiring no mounting hardware. The model 566010 is 1.22-in. tall, has four mounting clips, and suits medium-power devices. The model 530510 is 0.62-in. tall and suits low-power applications. PC-board soldering tabs are available for increased sturdiness. $0.44 (5000). **Aavid Engineering**, Laconia, NH. (603) 528-3400. **Circle No. 375**

Custom membrane-switch panel drops in. The Series 70 custom membrane switches feature a drop-in panel. The switch panel has an accompanying pc board that is 9 to 22.5 mm behind the front panel, depending on switching functions. LED-illuminated switches are optional. $8 to $10 per function. **EAO Switch Crop**, Milford, CT. (203) 877-4577. **Circle No. 376**

IGBT modules shoulder greater amperages. The H-Series IGBT modules now handle 300 and 400A at 600V using the same-sized package as did the previous 200 and 300A units, respectively. Despite the greater current-carrying capacity, case temperatures have not increased. The modules include a soft-recovery diode. $177.73 to $231.04. **Powerex Inc**, Youngwood, PA. (412) 925-4422. **Circle No. 377**

Connectors mate to miniature valves. The GDS series connectors mate with DIN 43650 Form C miniature valves used for industrial control. Female cable-mount and male panel-mount versions are available with solder or screw-wire attachments. The connectors have an IP 65 rating (suitable for hose-down and spray environments). $1.32 (1000). **Richard Hirschmann of America**, Riverdale, NJ. (201) 835-5002, ext 230. **Circle No. 378**

Aluminum capacitors deliver peak currents to high-power audio amplifiers. The Boomer-Cap line of aluminum capacitors suits professional audio amplifiers have outputs as high as 10 kW pk. The 1.2F units measure 3×8⅝ in., and 1F units measure 3×5⅝ in. Rated for 10-kA pk cur-

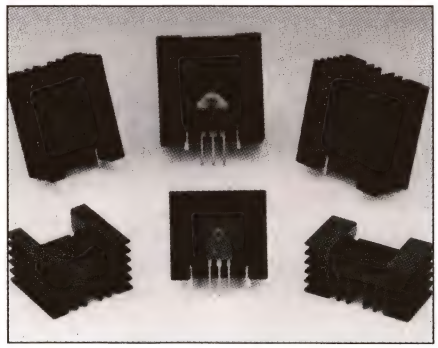
rents, the capacitors are an outgrowth of Strategic Defense Initiative research. Their voltage rating is 20V. $35. **Cornell Dubilier**, Pickens, SC. (803) 878-6311. **Circle No. 379**

Touch screen plugs into multimedia players. The Crystal Clear touch screen for multimedia players connects using either an 8- or 9-pin "RS-232-C" connector. Versions are available for Philips Consumer Electronics CD-I 220 and 604 CM135 monitors and other popular multimedia monitors. $495. **Interaction Systems Inc**, Watertown, MA. (617) 923-6001. **Circle No. 380**

Fuseholders meet IEC requirements. The FPG series fuseholders for 5×20-mm fuses meet the power-dissipation requirements of IEC 127-6,PC2. Panel-mount versions handle 4W; pc-board versions handle 2.5W. The series also meets the shock-safety requirements of IEC 529. The units' materials meet UL94V-O with an oxygen index of 31% and a comparative tracking index of 275. The series is insert molded for a complete seal at its base, suiting potted applications. Tab or solder connections are available. Panel-mount versions also have a front seal. UL and CSA rate the fuseholders for 16A at 250V (10A at 250V by VDE, SEMKO, and SEV). Fuseholders, $0.82 (500). Delivery is from stock. **Schurter**, Petaluma, CA. (707) 778-6401. **Circle No. 381**

Micromachined accelerometers feature response to 2 kHz. A family of micromachined, surface-structure accelerators comes in 10, 25, 50, and 100g versions. The units come in 20-pin leadless chip carriers (LCCs). The model 1010 outputs a digital pulse stream whose rep rate is proportional to acceleration. The model 1210, operating from 5V, provides a ±3V analog output. The unit has a 100-dB range. The model 1100 threshold accelerometer generates a logic output when acceleration exceeds a threshold. Operational temperature range is –55 to +125°C. Model 1010 LCC, $59; J-lead, $64 (1000). **Silicon Designs Inc**, Issaquah, WA. (206) 391-8329. **Circle No. 382**

Data-access arrangement meets Japanese specs. The CH1817J family of data-access arrangements (DAAs), meets Japan Approvals Institute of Telecommunications Equipment (JATE) and Ministry of Posts and Telecommunications specifications. The units are compatible with modem and fax chip sets, including V.32bis through V.TURBO and V.FAST. Single-ended and differential models are available. $15. **Cermetek Microelectronics**, Sunnyvale, CA. (408) 752-5000. **Circle No. 383**



Heat sinks cool TO220, 218, TO3-P, and multiwatt devices. A family of 1.65 and 2-in.-wide heat sinks mounts vertically and provides a threaded mounting hole. You can mount the heat sinks with tin-plated solderable studs or screws. $1 (1000); delivery is three to four weeks ARO. **International Electronic Research Corp**, Burbank, CA. (213) 849-2481. **Circle No. 384**

Space-rated, battery-cell-bypass switch prevents power loss after individual cell's failure. The model 1176 cell-bypass switch senses a cell's failure in a battery, automatically bypassing the failed cell. The switch detects cell-leakage current and uses one or two electromechanical actuators to handle as much as 300A. Switch operation occurs without shock, vibration, or debris. Model 1176, $1950 typ (50); delivery, 12 weeks ARO. **G&H Technology Inc**, Camarillo, CA. (805) 484-0543. **Circle No. 385**

Semiconductor laser's emission matches HeNe gas lasers'. The HL6312G solid-state laser diode produces a 5-mW, 630-nm output, which is the same wavelength as HeNe gas lasers'. Typical operating specs are 2.7V at 65 mA, suiting battery-powered applications. The unit's operating lifetime is 1000 hr at 5 mW and 50°C. $79 (1000). **Hitachi America Ltd**, Brisbane, CA. (415) 589-8300. **Circle No. 386**

500-MHz solid-state switch has 8Ω on-resistance and 10-pF on-capacitance. The DG643 single-pole, double-throw analog switch handles 75 mA. The units come in small-outline, surface-mount packages. 16-pin plastic DIP, $1.80; SO-16, $1.96 (1000). **Siliconix**, Santa Clara, CA. (408) 988-8000. **Circle No. 387**

Electrolytic-capacitor mountings protect capacitors and facilitate pc-board cleaning. The ECM series of electrolytic-capacitor mountings allow venting and proper draining during pc-board cleaning. The units are made from UL-rated 94V-2 nylon per ASTM D4066 PA111 and raise the capacitor 0.050 in. above the pc board. The mountings ease inspection and protect the caps from shock, vibration, and accidental lead bending. $44.50 per 1000 (10,000). **Bivar Inc**, Irvine, CA. (714) 951-8088. **Circle No. 388**

High-brightness green, amber, and red LEDs illuminate large-area displays. High-brightness LEDs radiate in a 60°-horizontal and 30°-vertical pattern, which is twice the viewing angle of conventional high-brightness LEDs. The 570-nm, 270-mcd HLMP-V500 costs $0.28; the 592-nm, 460-mcd HLMA-VL00 costs $1.07; and the 644-nm, 1000-mcd HLMA-V100 costs $0.72 (1000). All versions come in T-1$^{3}/_{4}$ untinted, nondiffused packages. **Hewlett-Packard Co**, Santa Clara, CA. (800) 537-7715, ext 7939. **Circle No. 389**

Telecommunications-relay series meets 2500V Bellcore specification for voltage-surge isolation. The FBR10 telecommunications-relay series measures 0.2×0.1 in. and consumes 140 mW when energized. The units switch 220V dc or 250V ac max at 2A max. The units perform 200,000 operations at 30V dc, 1.5A resistive. The devices come in a 12-pin DIP with two form-C contacts. $3.47. **Fujitsu Microelectronics Inc**, San Jose, CA. (408) 922-9000. **Circle No. 390**

PCMCIA connector is smaller and thinner than its predecessors. The IC7 series of 68-pin connectors suits PCMCIA Type I, II, and III memory cards. The units are through-hole or surface mountable (either side of a pc board) and offer a choice of left or right eject buttons. The units have 1.27-mm contact spacing. They measure 85× 65×5.4 mm. $4.50 (1000). **Hirose Electric Inc**, Simi Valley, CA. (805) 533-7958. **Circle No. 391**

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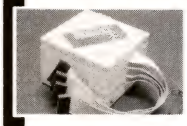

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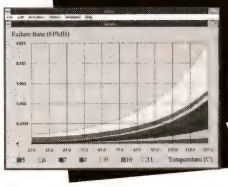

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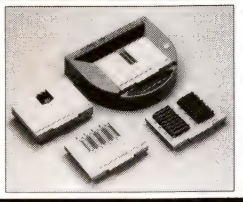

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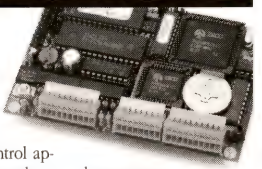

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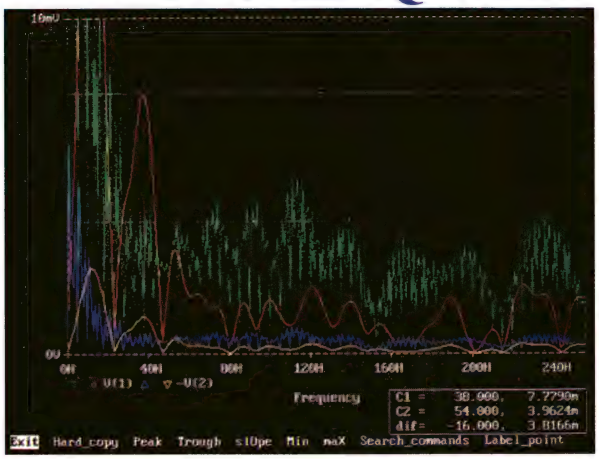

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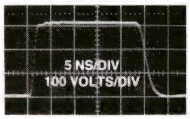

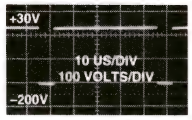

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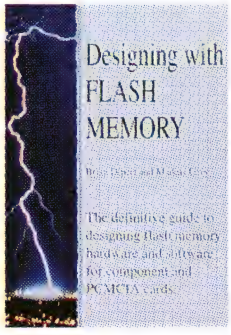

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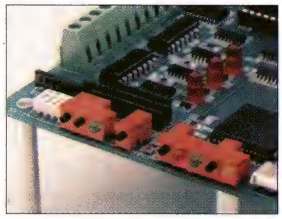

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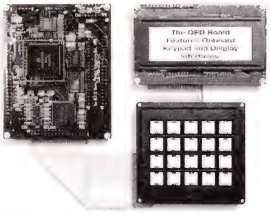

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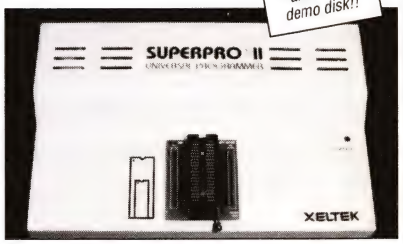

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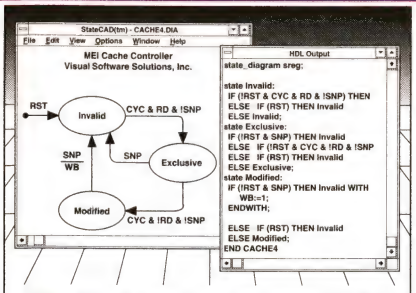

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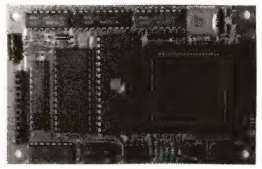

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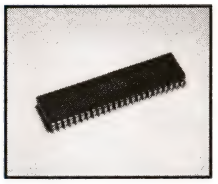

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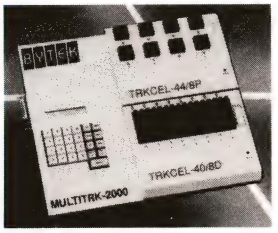

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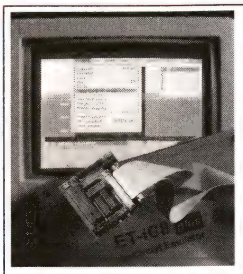

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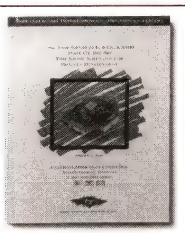

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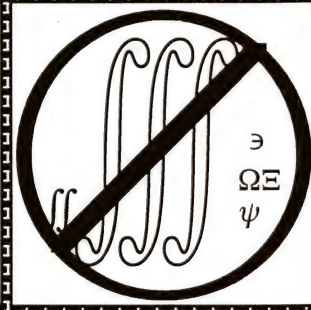

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Candidates must also have a BS in Computer Science or Computer/Electrical Engineering (MS preferred) and 8 years experience to include 2 years of task/project leadership. Software development in a PC environment is a must.

CSC offers competitive salaries and benefits. Please mail resumes in confidence to: **CSC/ATD/Langley, 3217 North Armistead Ave., Hampton, VA 23666-1379. FAX: (804) 865-1725.** An Equal Opportunity Employer M/F/D/V.

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Utilize your circuit design and software development experience to assume total engineering project responsibility in a fasted paced, team oriented environment. Test Engineers at Jabil Circuit are expected to perform the full range of activities related to the design, development and implementation of In-Circuit, Functional, ESS and customer supplied test programs. This includes the design of a wide variety of test fixtures, as well as reducing the cost and improving the functionality of assigned assemblies. The successful candidate will possess a BSEE and related software experience in "C" and Assembly level programming. Strong communication skills are a must.

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Develop and implement network based system level diagnostic test processes. Provide technical leadership to identify and resolve complex hardware/software/firmware system anomalies. Customize system level testing and reporting to accommodate various customer and business requirements.

In return for your expertise, we provide a competitive salary and benefits package along with a state-of-the-art work environment. For confidential consideration, please call or send resume to the **Human Resources Department at 10800 Roosevelt Boulevard, St. Petersburg, FL 33716. (813)576-5091.**

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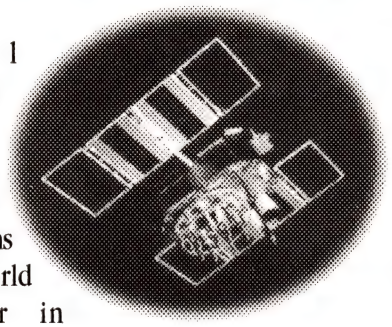
GPS SOFTWARE ENGINEERS



Rockwell International Corporation's Collins Avionics & Communications Division, a world class leader in electronics and technology for communications, guidance and control has a number of challenging engineering opportunities at our Cedar Rapids, IA facility.

Software Engineering Requirements

- Embedded real-time avionics software development experience
- Design, code, test, verification experience
- High-level languages
- BSCS/BSEE required
- A minimum of two years GPS experience preferred
- Must be able to work in a team-oriented environment

U.S. citizenship is required. Applicant selected will be subject to security investigation and must meet eligibility requirements for access to classified information. Successful candidates will be required to pass a drug screen test.

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The new generation in digital television has triggered a revolution in telecommunications. At the forefront of this revolution is General Instrument Corporation, the world's largest supplier of access control, scrambling and descrambling equipment used by cable and satellite television programs, such as CNN, HBO, superstations and sports channels. We are a leader in the next generation of multi-channel digital and television technology High Definition Television (HDTV) and an integral part of the "Grand Alliance", which is combining technologies to become the U.S. broadcast standard for HDTV.

We have the following career opportunities for qualified professionals with the vision to enhance our future...and change the way the world sees itself.

SYSTEMS ENGINEERS

Will design advanced digital communications systems for satellite, cable and broadcast TV. Requires an MSEE plus at least 5 years' experience in the following areas: communication system design, system architecture, data communication protocols, telephony and networks, encryption and access control, digital signal processing, communication networks, digital video compression, satellite communications or system test/evaluation. (CODE PMN)

TEST ENGINEERS

Will develop test strategy and dedicated equipment used in production of complex consumer audio/video gear, and work from design phase through production start to optimize product design-for-test, test equipment design and product quality. Requires BSEE with 3-7 years' experience designing and/or programming dedicated test equipment and associated products. Exposure to Boundary-Scan, NTSC/PAL testing and GenRad test equipment is highly desirable. Openings exist in hardware and firmware; must have skills in both. (CODE MMN)

FIRMWARE ENGINEERS

Will design, develop and integrate embedded real-time code for complex video scrambling/compression systems. Requires a BSEE with experience in firmware design and microprocessor/controller real-time programming. Familiarity with communication theory and firmware test development is a plus. (CODE JPN)

DIGITAL DESIGN ENGINEERS

Will design a variety of digital compression boards and perform signal processing developmental tasks encompassing field programmable gate arrays and microprocessor-based systems. Duties will also include system integration/test and involvement from product conception to production. Requires a BSEE (MSEE desirable) and 3+ years' experience, along with strong skills in UNIX, Viewlogic and FPGA (XILINX, ACTEL, MAX). (CODE LTN)

ANALOG/RF DESIGN ENGINEERS

Will design analog/RF circuits and systems for video/audio hardware. Detail design includes op-amp, transistor circuits, oscillators, A/D, D/A, filters, PLL and amplifiers. Requires analog/RF design experience (DC thru UHF); MSEE and video/audio circuit design a plus. (CODE HSN)

PRODUCT DEVELOPMENT ENGINEERS

Will design sophisticated products for DigiCipher-II video systems. Positions are available for Project, Lead and Design Engineers. All products encompass a broad range of technologies including digital demodulation, error correction, video and audio decompression, advanced GUI, and DES-based access control. Transmission is via MPEG-2 compatible packet bit stream. Requires BSEE (minimum) with 4+ years' experience in analog/digital hardware design, hardware/firmware integration and communications systems. (CODE BDN)

SOFTWARE ENGINEERS

Will design, develop and integrate program modules utilizing "C" on VAX/VMS platforms, Record Management Services (RMS) and low-level screen interface routines to handle Man Machine Interface (MMI) transaction processing and file management for satellite TV applications such as access authorization, feature control, on-screen text, etc. Requires a BSCS or related degree with software engineering design/code experience in a multi-tasking environment. (CODE NLN)

The world is watching what we do. Be part of this new wave of technology. Send your resume including salary history/requirements, referencing appropriate code to: Human Resources, General Instrument Corp., 6262 Lusk Blvd., San Diego, CA 92121. On-site gym. Smoke-free facility. EOE.

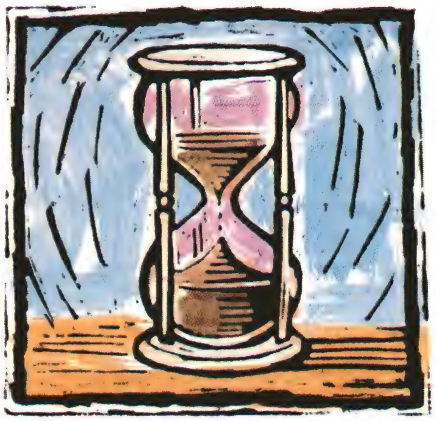
GI General Instrument

DESIGN ENGINEER **8 am to 5 pm**
$17.35/hr **40 hours per week**

Design and development of embedded controller software. Research and design of signal processing algorithms. Master of Science degree, major in Electrical Engineering or equivalent. Two (2) years experience in job offered or two (2) years experience as engineer/scientist. Experience must have included 12 months of "C" language usage and real time system programming and graphics programming. Contact LA Office of Employment Security, Job Order 093762, 1991 Wooddale Blvd., Baton Rouge, LA 70806.

1. THIS NOTICE IS PROVIDED AS A RESULT OF THE FILING OF AN APPLICATION FOR PERMANENT ALIEN LABOR CERTIFICATION.
2. ANY PERSON MAY PROVIDE DOCUMENTARY EVIDENCE BEARING ON THE APPLICATION TO LOUISIANA DEPT. OF LABOR, ALIEN LABOR CERTIFICATION UNIT, RM. 110, P.O. BOX 94094, BATON ROUGE, LA 70804-9094 and/or REGIONAL CERTIFYING OFFICER, U.S. DEPARTMENT OF LABOR, 525 GRIFFIN STREET, ROOM 314, DALLAS, TX 75202.

TECHNOLOGY UPDATE
April 25-29, 1994
Monterey, CA 93943-5110
POC: Dr. R. Panholzer,
Naval Postgraduate School
408-656-2948, Fax # 2816



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OUR ADVANCED LASER AND COMPUTER

for that is

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the stuff

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life is made of."

-Franklin

By giving physicians the means to diagnose disease in a matter of minutes and initiate treatment, Coulter's instruments and technologies impact the lives of thousands of people all over the world.

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Actual Size

Advancing the State-of-the-Art for Board-Mounted Converters.

Throwing out all the old design concepts, Power Trends has advanced the state-of-the-art again. This time it's for board-mounted DC-DC converters. By using switching frequencies greater than 650 kHz, planar magnetics and surface-mount construction—we have now produced the industry's smallest and most reliable 15 Watt isolated DC-DC converters.

Not only are the new products much smaller than competitive designs, but—with fewer components—they also significantly advance product reliability.

FEATURING

- **Smallest footprint: 1.45" x 1.64" x 0.38"**
- **Wide input voltage range: 36V to 72V**
- **80% efficiency**
- **Temperature range: -25°C to +70°C**
- **500 VDC isolation**
- **Planar magnetics**

Three products are initially available—the PT3101A, a 48V-to-5V unit; the PT3l02A, a 48V-to-l2V unit; and the PT3103A, a 48V-to15V unit. All three products operate over an input voltage range of 36 to 72 VDC and provide their rated power up to 70°C without additional heatsinks. They provide 80% efficiency, 500 VDC isolation, and are ideally suited for telecom, industrial, computer, medical, and other distributed-power applications requiring input-to-output isolation.

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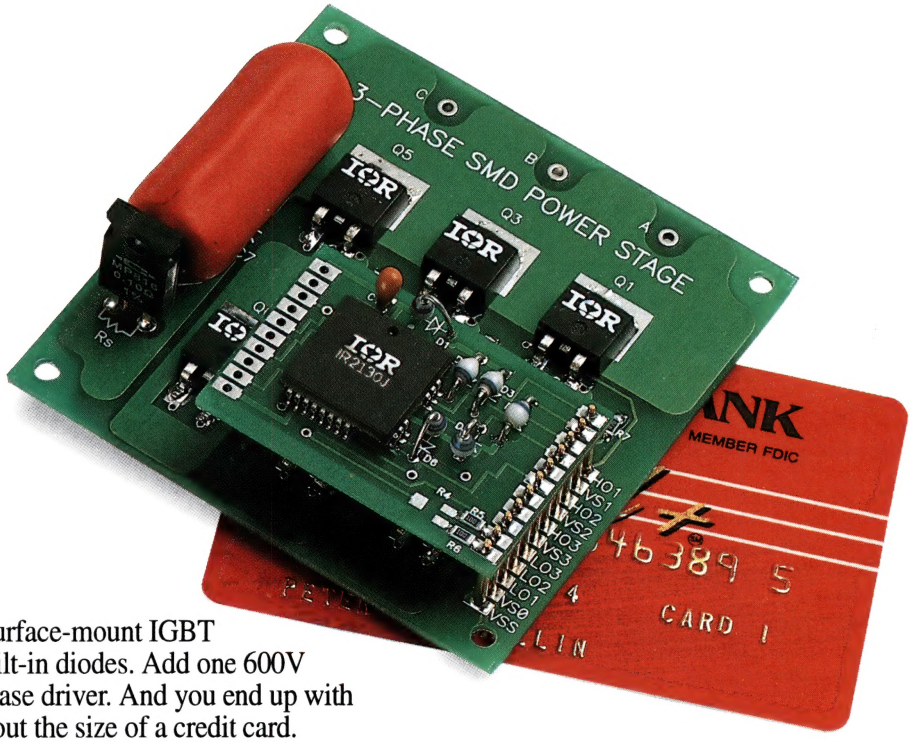
CIRCLE NO. 100

Power-full tiny inverter.

Or how to shrink a 1hp, 3-phase motor control inverter to fit your pocket...book.



This motor control inverter is 3" x 3" sq. and features six SMD-220 surface-mount CoPack UltraFast IGBTs driven by a single 600-volt, 3-phase driver (IR2130J) with current-sensing.

Take six IR surface-mount IGBT *CoPacks* with built-in diodes. Add one 600V IR2130J three-phase driver. And you end up with a 1hp inverter about the size of a credit card.

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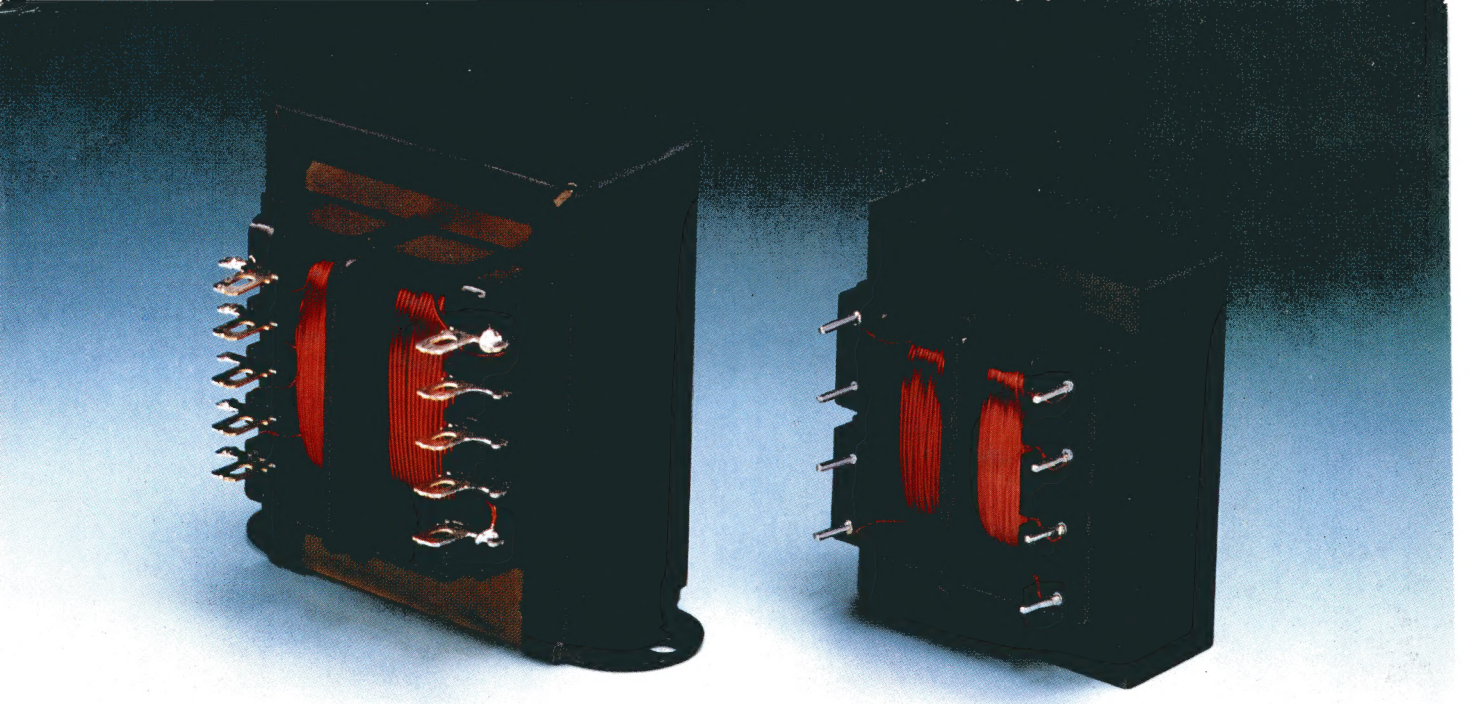


TRANSFORMERS FOR CLASS 2 APPLICATIONS

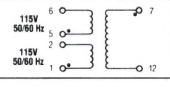
DUAL BOBBIN DESIGNS FEATURE 4000 VRMS PRIMARY AND SECONDARY ISOLATION.

*INHERENTLY LIMITED
**NON-INHERENTLY LIMITED
MAXIMUM FUSE VALUE SPECIFIED

ALL PRIMARIES ARE 115/230 VOLT 50/60 HZ

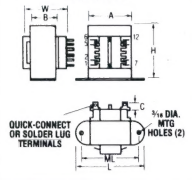
PART NO.	SECONDARY RMS RATING	FUSE REQD.	PRICE
CL2-25-12	12V @ 2.10A	2.5A**	14.50
CL2-25-24	24V @ 1.05A	N/A*	14.50
CL2-40-12	12V @ 3.33A	4.0A**	18.50
CL2-40-24	24V @ 1.66A	2.0A**	18.50
CL2-80-24	24V @ 3.33A	4.0**	25.25

SCHEMATIC

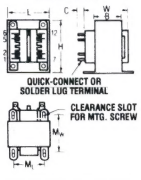


PRIMARIES ARE DESIGNED TO BE USED SIMULTANEOUSLY THAT IS, THEY MUST BE USED EITHER SERIES OR PARALLEL CONNECTED (AS ONE WINDING).

MTG. STYLE C



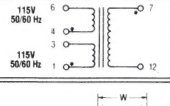
MTG. STYLE B



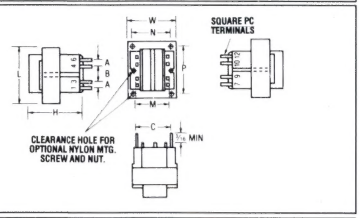
DIMENSIONS								Mtg.	Mtg.		Mtg.	
VA	L	W	H	A	B	C	Terminals	Style	ML	MW	Screw	Lbs.
25	2 13/16	1 7/8	2 5/16	2	1 1/8	5/16	3/16 (.187)	C	2 3/8	–	#6	1.25
40	3 1/8	2 1/16	2 11/16	2 1/4	1 1/8	5/16	3/16 (.187)	C	2 13/16	–	#6	1.6
80	2 1/2	2 3/8	3	–	1 3/8	5/16	3/16 (.187)	B	2	2 3/16	#6	2.8

PART NO.	SECONDARY RMS RATING	FUSE REQD.	PRICE
CL2-2.5-12	12V @ .20A	N/A*	9.00
CL2-2.5-24	24V @ .10A	N/A*	9.00
CL2-5.0-12	12V @ .42A	N/A*	9.75
CL2-5.0-24	24V @ .20A	N/A*	9.75
CL2-10-12	12V @ .83A	N/A*	10.90
CL2-10-24	24V @ .42A	N/A*	10.90
CL2-20-12	12V @ 1.66A	N/A*	13.25
CL2-20-24	24V @ .833A	N/A*	13.25
CL2-30-12	12V @ 2.50A	3.0A**	15.25
CL2-30-24	24V @ 1.25A	N/A*	15.25
CL2-50-12	12V @ 4.20A	5.0A**	18.65
CL2-50-24	24V @ 2.10A	2.5A**	18.65

SCHEMATIC



PRIMARIES ARE DESIGNED TO BE USED SIMULTANEOUSLY THAT IS, THEY MUST BE USED EITHER SERIES OR PARALLEL CONNECTED (AS ONE WINDING). (See mechanical drawing for correct footprint)



DIMENSIONS							Pin	Mtg.			Mtg. Screw		
VA	L	W	H	A	B	C	Dimensions	M	N	P	Size	Quantity	Lbs.
2.5	1 5/8	1 5/16	1 1/8	.200	.250	1.000	0.025SQ	1 1/16	–	–	#4	2	0.25
5.0	1 5/8	1 5/16	1 3/8	.200	.400	1.000	0.025SQ	1 1/16	–	–	#4	2	0.37
10.0	1 7/8	1 5/16	1 3/8	.200	.400	1.140	0.038SQ	1 1/4	–	–	#4	2	0.53
20.0	2 1/4	1 7/8	1 5/8	.400	.400	1.460	0.038SQ	1 1/2	–	–	#4	2	0.90
30.0	2 5/8	2 3/16	1 5/16	.550	.275	1.680	0.045SQ	–	1 3/4	2 3/16	#6	4	1.15
50.0	3	2 1/2	1 13/16	.600	.300	1.900	0.045SQ	–	2	2 1/2	#6	4	1.70

Signal's "**Class 2**" transformers feature the same dual high-temperature bobbin construction and insulating shroud originally developed for the company's very successful International Series. Available in both PC and chassis mount versions, they offer a choice of inherently limited or non-inherently limited designs and feature 4000 VRMS primary and secondary isolation.

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